INTEGRATED CIRCUIT APPLICATIONS

LECTURE NOTES

B.TECH
(III YEAR – I SEM)
(2018-19)

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OF ENGINEERING & TECHNOLOGY
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Unit I

Operational Amplifier

Operational Amplifier

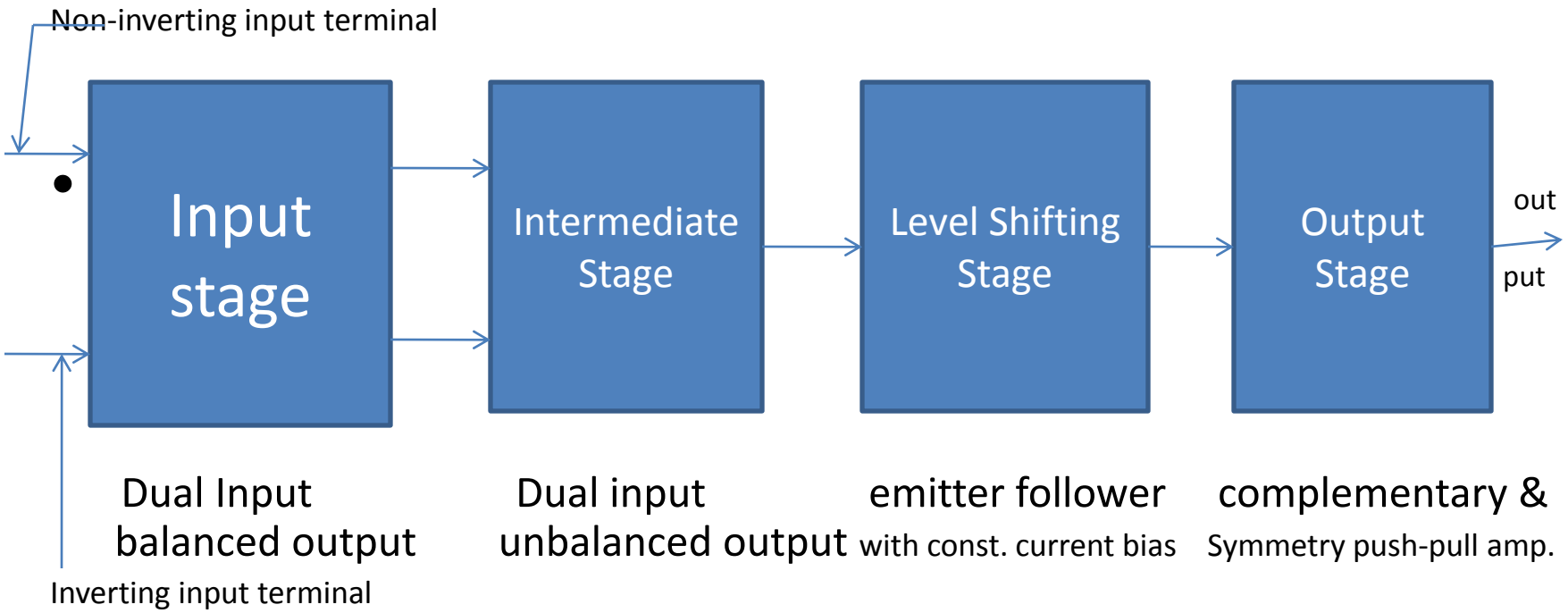
- An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifier and usually followed by a level translator and an output stage.
- An operational amplifier is available as a single integrated circuit package.
- The operational amplifier is versatile device that can be used to amplify DC as well as AC input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.

Operational Amplifier cntd..

- With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications such as AC and DC signal amplification, active filters, oscillator, comparators and regulators, and others

Block Diagram of Op-Amp

- Since an op-amp is a multi stage amplifier it can be represented by a block diagram as shown in the following figure.



Block Diagram of Op-Amp cntd…

- The input stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp
- Because of the direct coupling used, the DC voltage at the output of the intermediate stage is well above the ground potential. Therefore, generally, the level translator circuit is used after the intermediate stage
- The final stage is usually a push-pull complimentary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of op-amp. A well designed output stage also provides low output resistance.

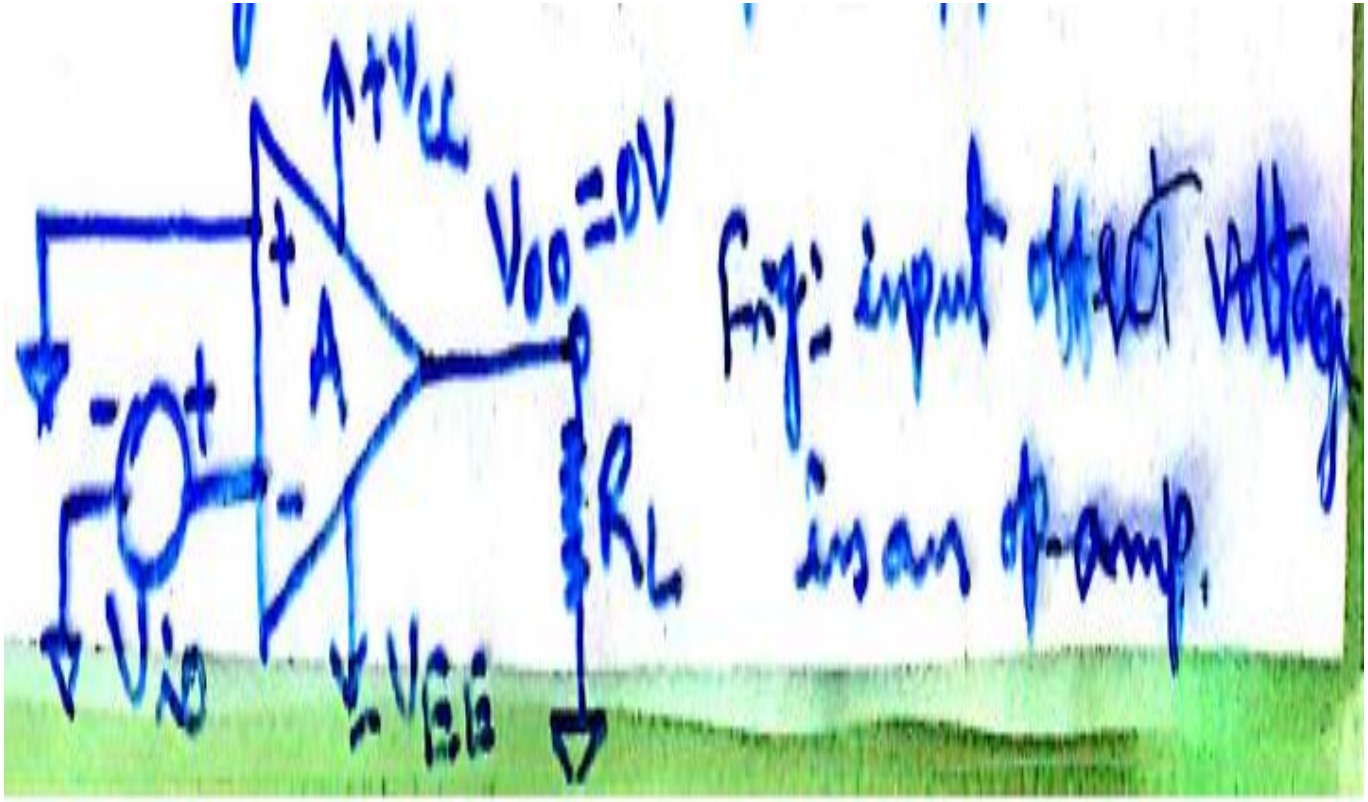
The IDEAL Op-amp

- An IDEAL op-amp would exhibit the following electrical characteristics.
  - Infinite voltage gain, A
  - Infinite input resistance Ri
  - Zero output resistance Ro
  - Zero output voltage when input voltage is zero.
  - Infinite bandwidth – any signal can be amplified without attenuation
  - Infinite common mode rejection ratio
  - Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

Practical Op-amp

- **Input offset voltage**: Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp with out any external inputs applied.

Practical Op-amp cntd…



Practical Op-amp cntd…

- **Output Offset Voltage:**
  - The output voltage caused by mismatching between two input terminals is called the output offset voltage Voo.
  - The output offset voltage Voo is a DC voltage, it may be +ve or –ve in polarity depending on whether the potential differences between the two input terminals is +ve or –ve.

Practical Op-amp cntd…

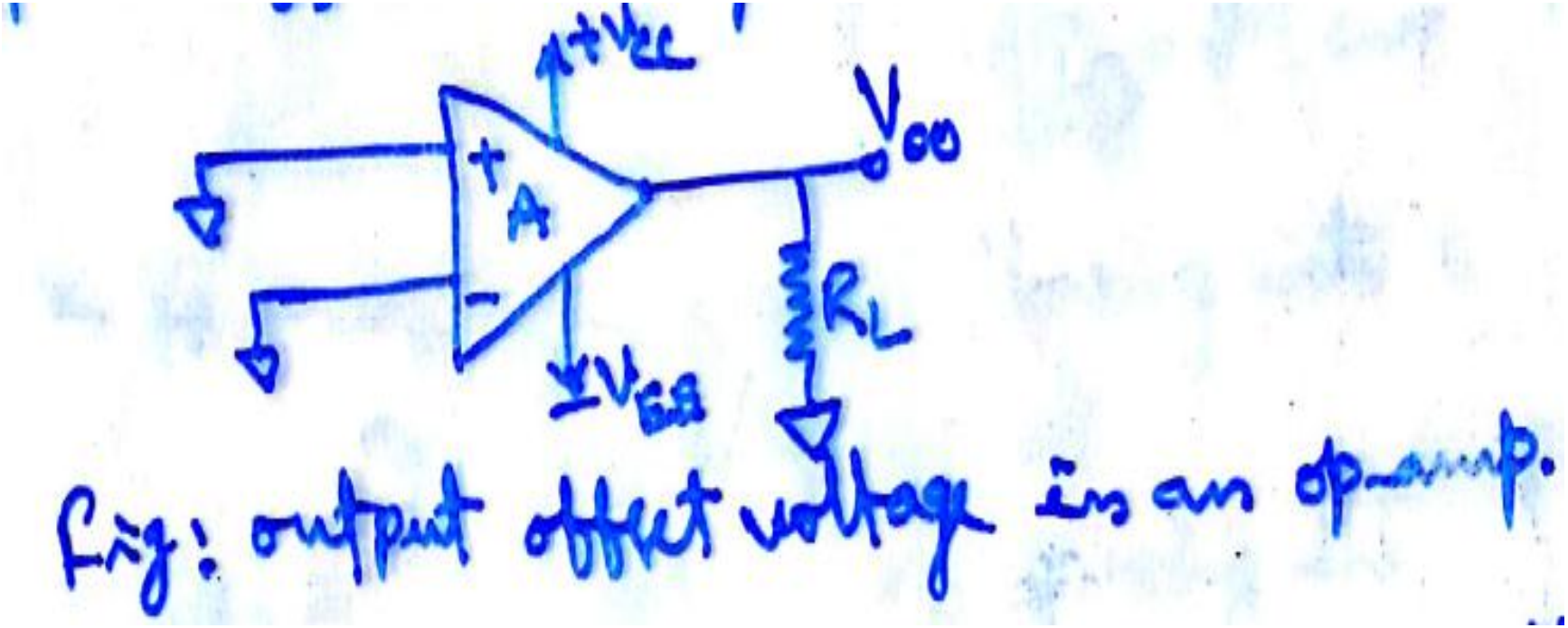


Fig: output offset voltage in an op-amp.

Practical Op-amp cntd…

- **Input offset Current:**
  - The input offset current Iio is defined as the algebraic difference between two input bias currents Ib1 and Ib2. In equation form it is

$$Iio = |Ib1 - Ib2|$$

Practical Op-amp cntd…

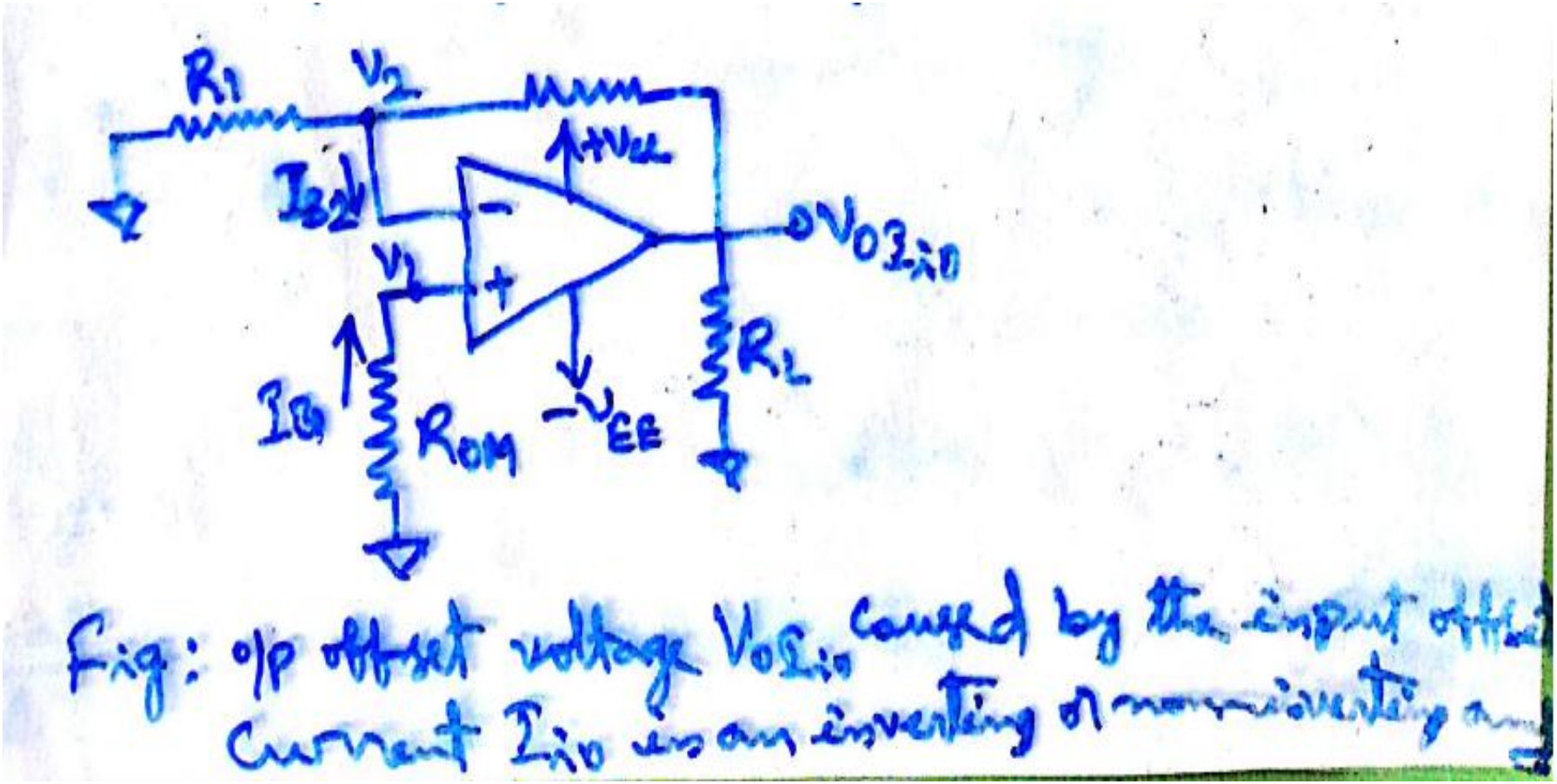


Fig: o/p offset voltage $V_{OS_{io}}$ caused by the input offset
Current I_{io} in an inverting or non-inverting

Practical Op-amp cntd…

- **Input Bias Current:**
  - An input bias current Ib is defined as the average of the two input bias currents, Ib1 and Ib2 as shown in the following figure.

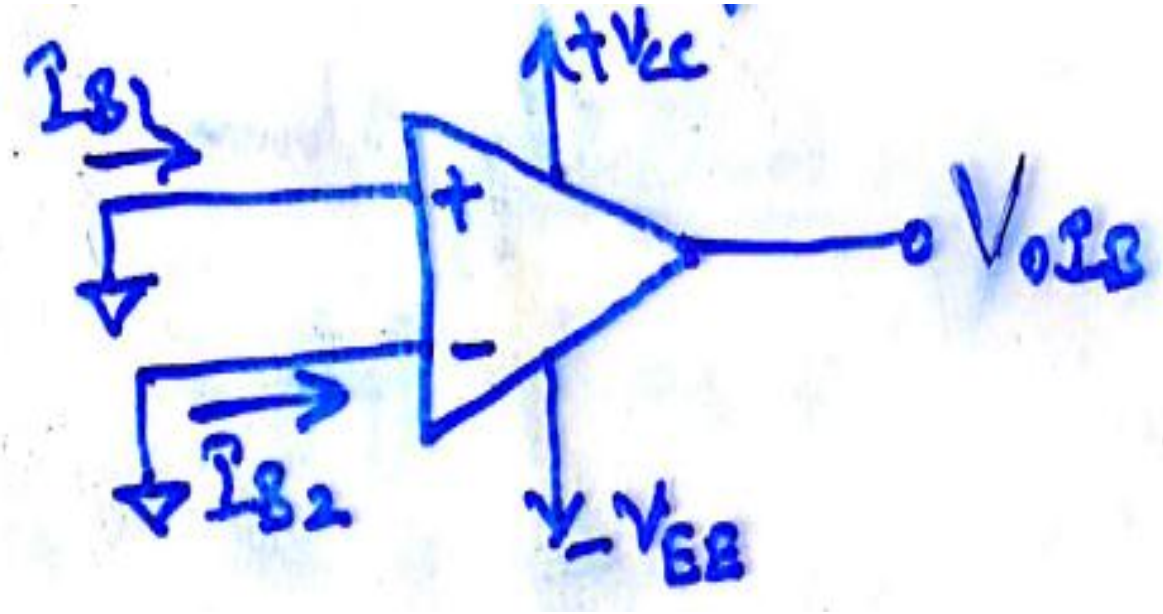
$$Ib = (Ib1 + Ib2)/2 \quad [Ib – DC\ current]$$

Where Ib1= DC bias current flowing into the non-inverting input

Ib2 = DC bias current flowing into the inverting input

- The value of input bias current Ib is very small, in the range of a few to few hundred nano amp.

Practical Op-amp cntd…



Practical Op-amp cntd…

- **Thermal Drift:**
  - The average rate of change of input offset voltage per unit change in temperature is called thermal voltage drift, and is denoted by $\Delta V_{io}/\Delta T$. Units – µV/°C
  - Similarly, the thermal drift in the input offset current & input bias current are defined as follows.
  - $\Delta I_{io}/\Delta T$= thermal drift in input offset current(pA/°C)
  - $\Delta I_b/\Delta T$= thermal drift in input bias current(pA/°C)

Practical Op-amp cntd…

- **Supply Voltage Rejection Ratio (SVRR) or Power Supply Rejection Ratio (PSRR):**
  - The change in op-amp's input offset voltage caused by variations in the supply voltages is called Supply voltage Rejection Ratio or Power Supply Rejection Ratio.
  - This is expressed either in microvolts per volt or in decibles
  - For example, SVRR for $\mu A741$ is ΔVio/ΔV=150 $\mu V/V$ maximum and it is 76.48 in DB.

Practical Op-amp cntd…

- **Common Mode Rejection Ratio (CMRR)**:
  - It can be defined as the ratio of the differential gain AD to the common mode gain Acm, that is CMRR = Ad/Acm
  - It is a measure of the degree of matching between two input terminals, that is, the larger the value of CMRR, the better is the matching between the two input terminals and the smaller is the output common mode voltage Vocm.

Differences b/w Ideal and Practical Op-Amp

Characteristics	Ideal Op-amp	Practical Op-amp
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Output voltage when input voltage is zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

Characteristics of Op-amp

- **DC Characteristics:** DC Characteristics include input bias current, input offset current, Input offset voltage, Output offset voltage and Thermal drift.
- **AC Characteristics:** AC characteristics include
  - Frequency Response
  - Slew Rate

Characteristics of Op-amp cntd…

- **Frequency Response:**
  - Ideally an op-amp should have an infinite band width.
  - The practical op-amp gain, however, decreases at higher frequencies.
  - What is the cause for the gain of the op-amp to roll-off after certain frequency is reached?
  - Obviously, there must be a capacitive component in the equivalent circuit of the op-amp. This capacitace is due to the physical characteristics of the device(BJT or FET) used and internal construction of op-amp.
  - For an op-amp with only one break frequency, all the capacitor effects can be represented by a single capacitor C as shown in figure 3.4 (a).

Characteristics of Op-amp cntd…

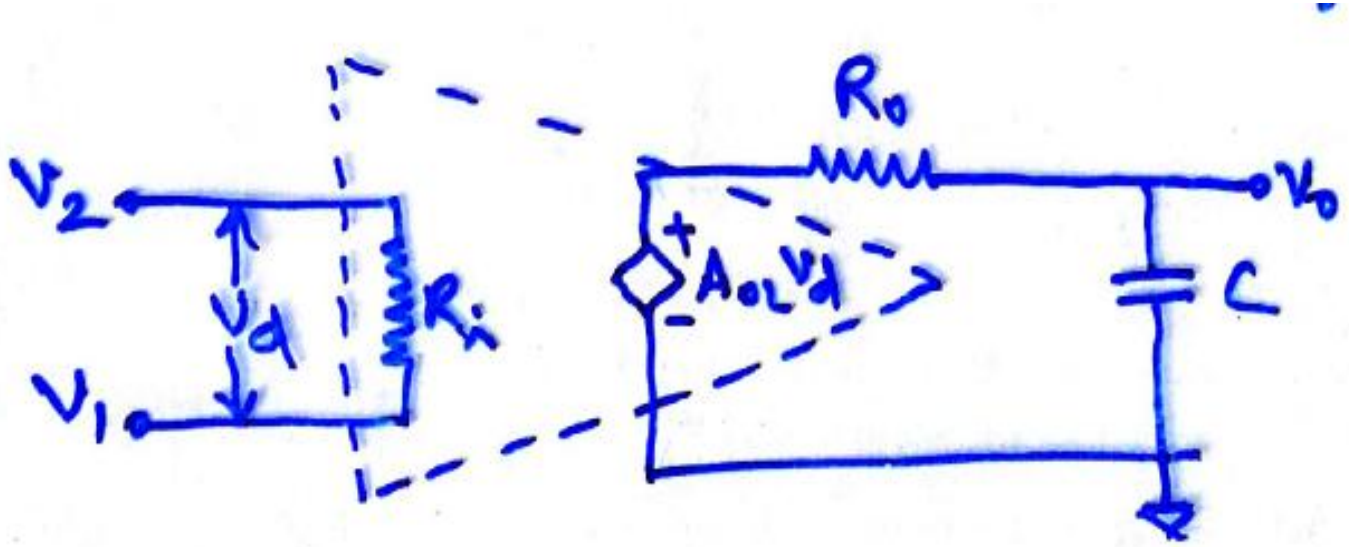


Fig 3.4(a) High frequency model of an op-amp with single corner frequency.

Characteristics of Op-amp cntd…

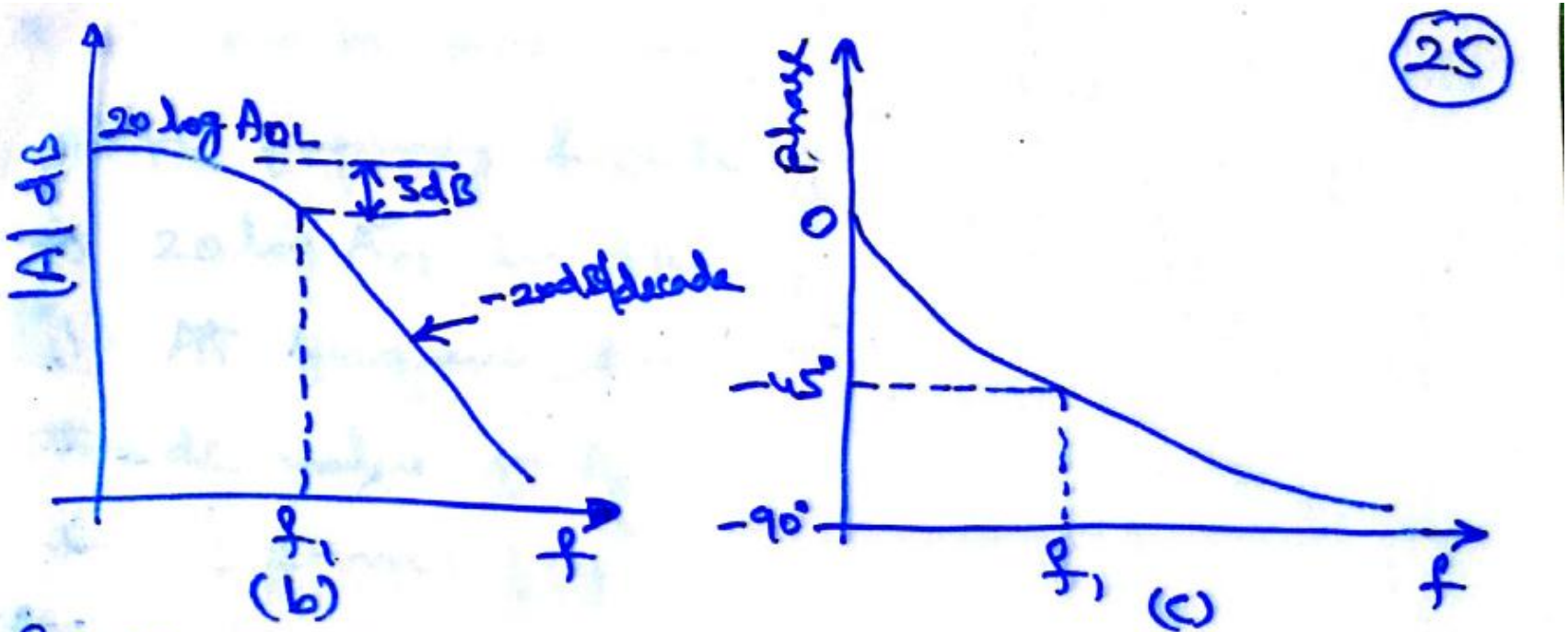


Fig 3-4 (b) open loop magnitude characteristics (c) phase characteristics for a op-amp with single break freq.

Characteristics of Op-amp cntd…

- The open loop voltage gain of an op-amp with only one corner frequency is obtained from Figure 3.4(a) as

  $V_o = -j X_c/(R_o - jX_c) A_{ol} V_d$

  $\Rightarrow A = V_o/V_d = A_{ol}/(1 + j2\pi f R_o C)$

  $A = A_{ol}/(1 + jf/f_1)$ where $f_1 = 1/2\pi R_o C$
- f_1 is the corner frequency or the upper 3 dB frequency of the op-amp.

Characteristics of Op-amp cntd…

- The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

  $|A| = A_{ol}/(\sqrt{(1+(f/f1)^2)}$ $\phi = -\tan^{-1}(f/f1)$

these are shown in Fig 3.4(b) and 3.4 (c)

- It can be seen that
  - For frequency f<<f1, the magnitude of the gain is 20 log Aol in dB.
  - At frequency f = f1, the gain is 3 dB down from the DC value of Aol in dB. This frequency f1 is called corner frequency
  - For f>>f1, the gain rolls off at the rate of -20dB/decade.

Characteristics of Op-amp cntd…

- It can further be seen from the phase characteristics that the phase angle is zero at frequency f=0.
- At corner frequency f1, the phase angle is -45° and at infinite frequency the phase angle is -90°. This shows that a maximum of 90° phase change can occur in an op-amp with a single capacitor.

Characteristics of Op-amp cntd…

- **Slew Rate:**
  - The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro seconds. In equation form, SR = (dVo/dt)|maximum V/µs.
  - Slew rate indicates how rapidly the output of an op-amp can change in response to changes in the input frequency.
  - One of the drawbacks of the 741C is it's low slew rate(0.5 V/µs), which limits its use in relatively high frequency applications, especially in oscillators, comparators and filters

Characteristics of Op-amp cntd…

- In high-speed op-amps especially, the slew rate is significantly improved. For instance, the LM138 has a slew rate of 70 V/µs.
- What causes the slew rate? There is usually a capacitor with in or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input.
- The rate at which the voltage across the capacitor Vc increases is given by dVc/dt = I/C. Here, I is the maximum current furnished by op-amp to the capacitor C. This means that for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor.
- For the 741C, that maximum internal capacitor charging current is limited to about 15 µA. So the slew rate of 741C is

  $SR = dVc/dt|max = Imax/C = 15\ \mu A/30\ PF = 0.5\ V/\ \mu s.$

741 Op-amp and it's features

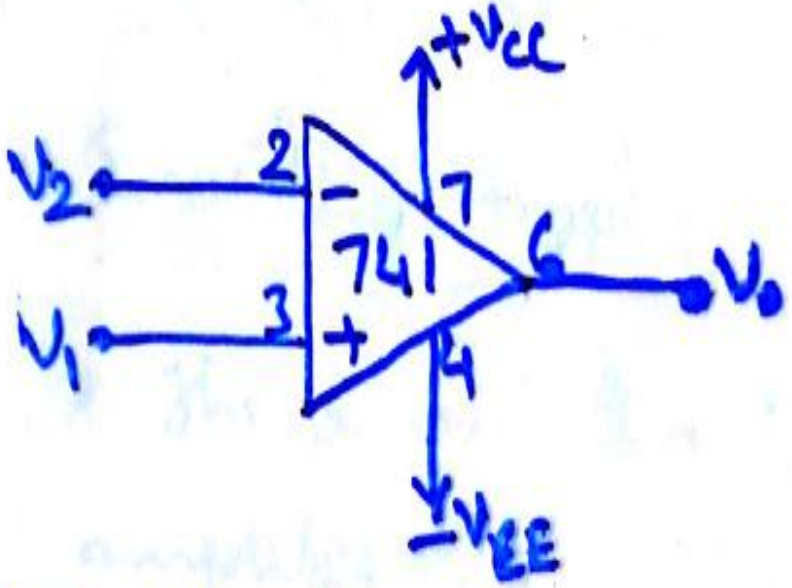


Fig (a) Simple 741 op-amp ckt

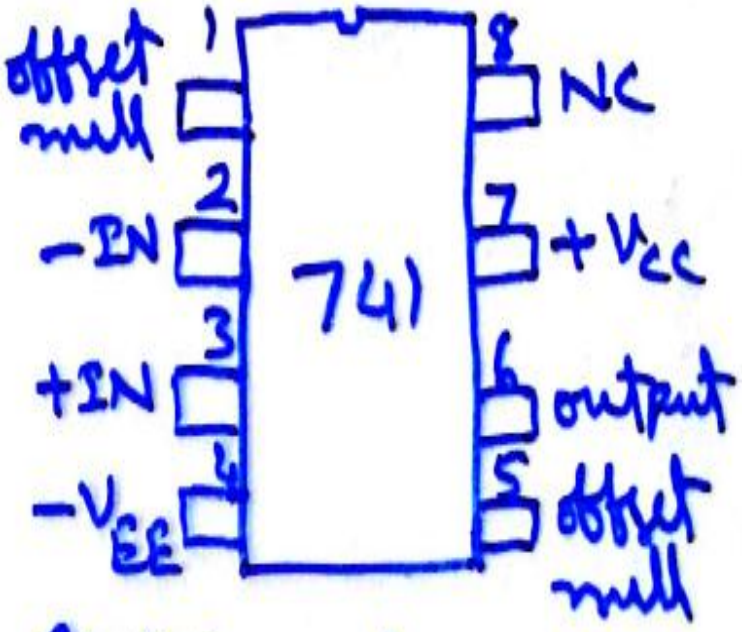


Fig (b) pin diagram of 741

741 Op-amp and it's features cntd…

- The μA741 is a high performance monolithic operation amplifier constructed using the planar epitaxial process.

The op-amp features are given below

1. High common mode voltage range make the μA741 ideal for use as voltage follower.
2. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.
3. 741 is internally frequency compensated op-amp
4. 741 is available in all 3 packages viz 8-pin metal can, 10-pin flat pack, and 8 or 14 pin DIP.
5. Offset voltage null capability is available.
6. It consumes low power

Modes of Op-amp

- Basically there are 2 modes of op-amp. They are
  - Inverting Amplifier
  - Non-Inverting Amplifier

Inverting Amplifier

- There are two types of connecting inverting amplifier. They are
  - Open loop inverting amplifier
  - Closed loop inverting amplifier

Modes of Op-amp cntd…

Open Loop Inverting Amplifier

- The circuit diagram for the open loop inverting amplifier is shown in figure 1.

Modes of Op-amp cntd…

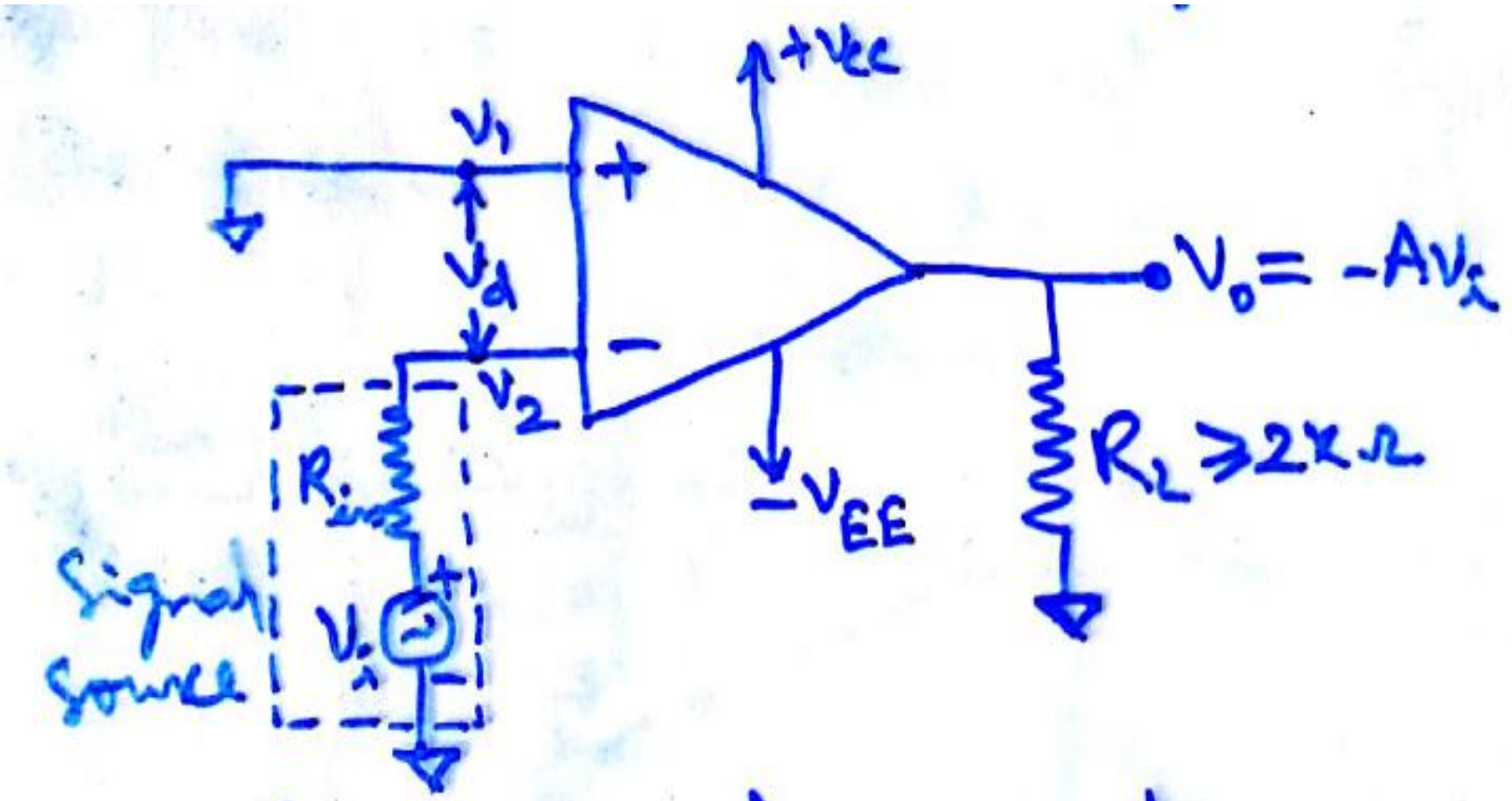


Fig 1. open loop inverting amplifier.

Modes of Op-amp cntd..

- The equation for the output voltage is given by

  $V_o = A(V_1 - V_2)$

  where A – large signal voltage gain

  V_1 – voltage at non-inverting input terminal

  V_2 – voltage at inverting input terminal

  here $V_1 = 0$ and $V_2 = V_i$ therefore

  $V_o = A(-V_i) = -A V_i$

- The negative sign indicates that the output voltage is out of phase with respect to the input by 180° or is of opposite polarity.
- Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output.

Modes of Op-amp cntd..

Closed Loop Inverting amplifier

- This is perhaps the most widely used of all the op-amp circuits.
- The circuit is shown in the figure 2(a)

Modes of Op-amp cntd..

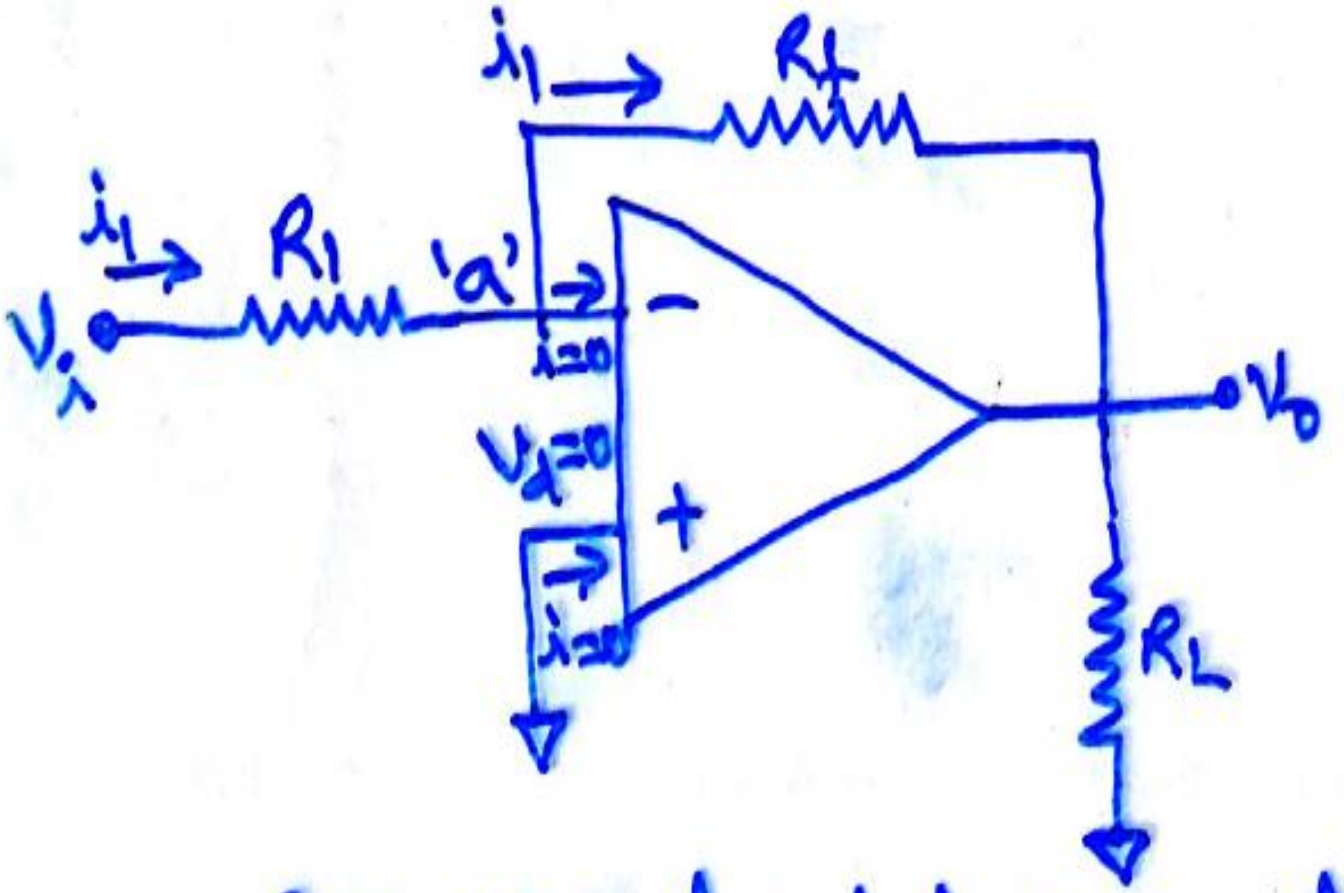


Fig 2(a) closed loop inverting amplifier.

Modes of Op-amp cntd..

- For simplicity, assume ideal op-amp. As Vd=0, node ‘a’ is at ground potential and the current i1 through R1 is $i1 = Vi/R1$
- Also since op-amp draws no current, all the current flowing through R1 must flow through Rf. Hence the output voltage is

  $Vo = -i1\ Rf = -(Vi/R1)\ Rf$

  therefore the gain of the closed loop inverting amplifier is $Acl = Vo/Vi = -Rf/R1$
- The –ve sign indicates a phase shift of 180° between Vi and Vo.

Modes of Op-amp cntd..

Example:

- In figure 2(b), R1 = 10KΩ, Rf = 100KΩ, Vi=1v. A load of 25 KΩ is connected at the output terminal. Calculate (i) I1 (ii) V0 (iii) il and total current io into the output pin

Modes of Op-amp cntd..

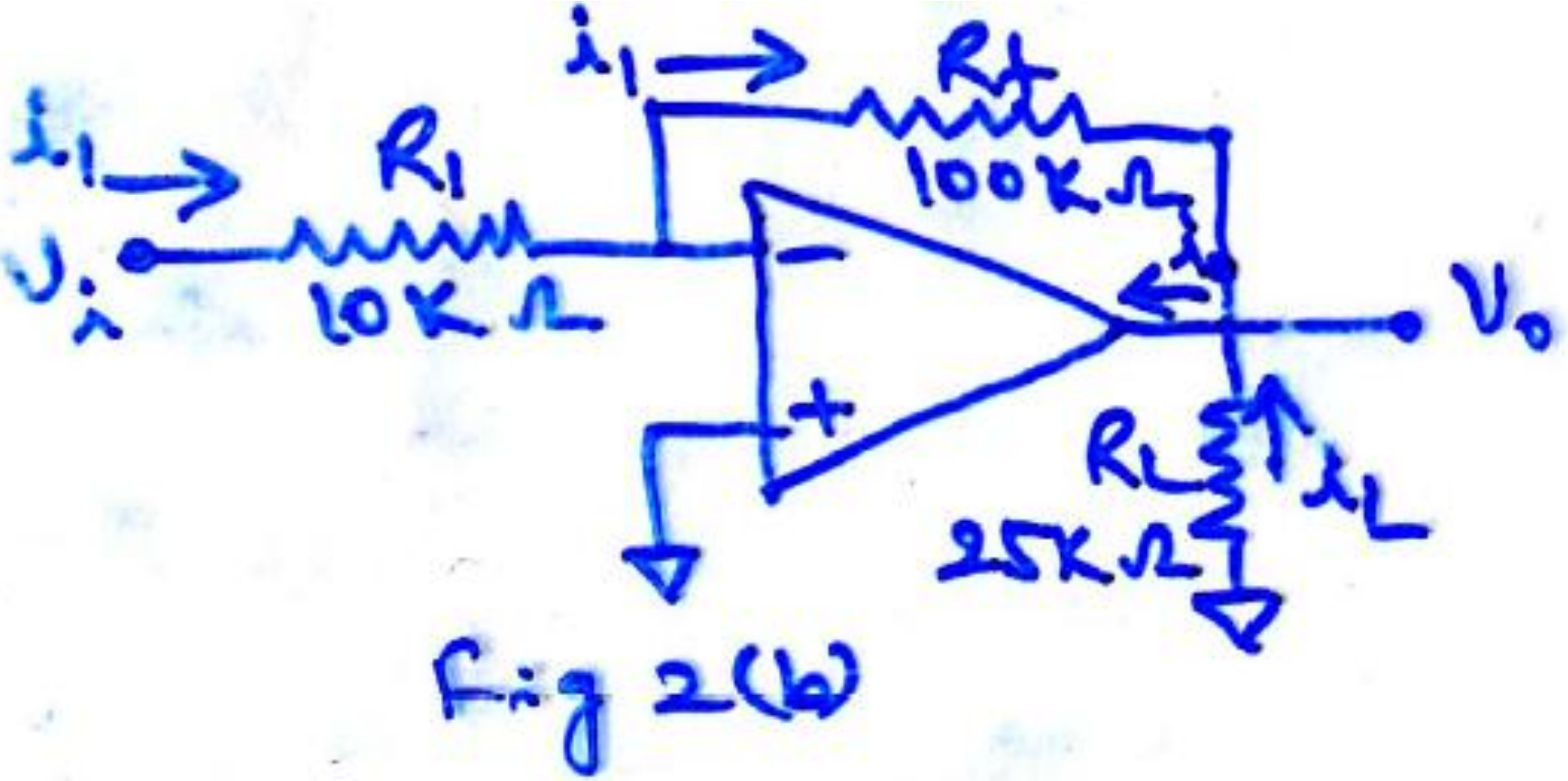


Fig 2(b)

Modes of Op-amp cntd..

(i) $i1 = Vi/R1 = 1V/10K\Omega = 0.1$ mA

(ii) $Vo = -Rf/R1\ Vi = -10V$

(iii) $il = -Vo/Rl = 10V/25\ K\Omega = 0.4$ mA

Therefore $Io = i1 + il = 0.1$ mA + 0.4 mA = 0.5 mA

Modes of Op-amp cntd..

Non-Inverting Amplifier:

- There are two types of connecting non-inverting amplifiers. They are
  - Open loop non-inverting amplifier
  - Closed loop non-inverting amplifier

Open Loop Non-inverting amplifier

- Figure 3.11 shows the open loop non-inverting amplifier

Modes of Op-amp cntd..

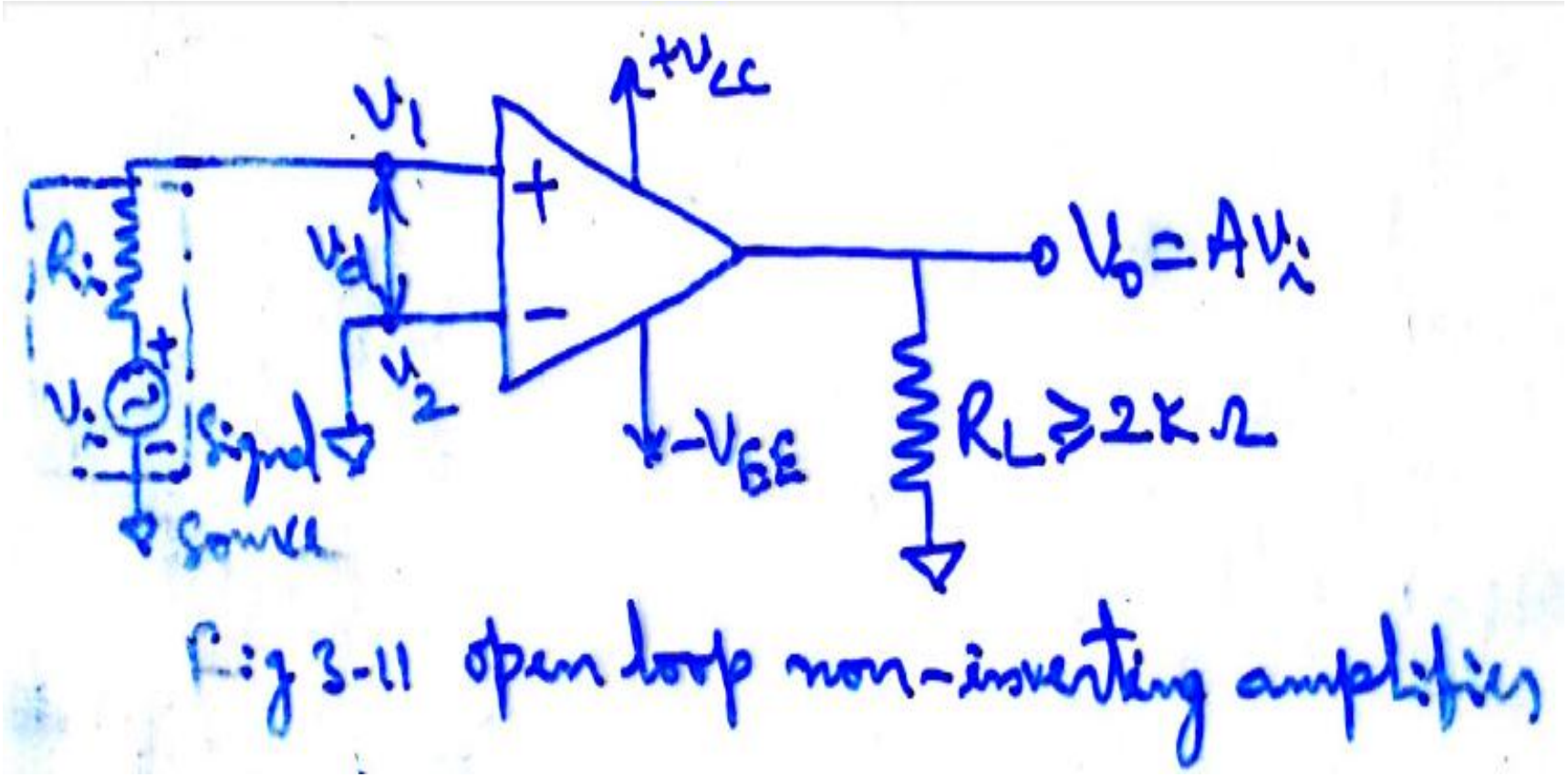


Fig 3-11 open loop non-inverting amplifier

Modes of Op-amp cntd..

- Output voltage, $V_o = A (V_1 – V_2)$

  here $V_1 = V_i$ and $V_2 = 0$ v

  therefore $V_o = A V_i$
- This means that the output voltage is larger than the input voltage by gain A and is in phase with the input signal.

Modes of Op-amp cntd..

Closed Loop Non-Inverting Amplifier:

- If the signal is applied to the non-inverting input terminal and feedback is given as shown in Figure 2.7(a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier.

Modes of Op-amp cntd..

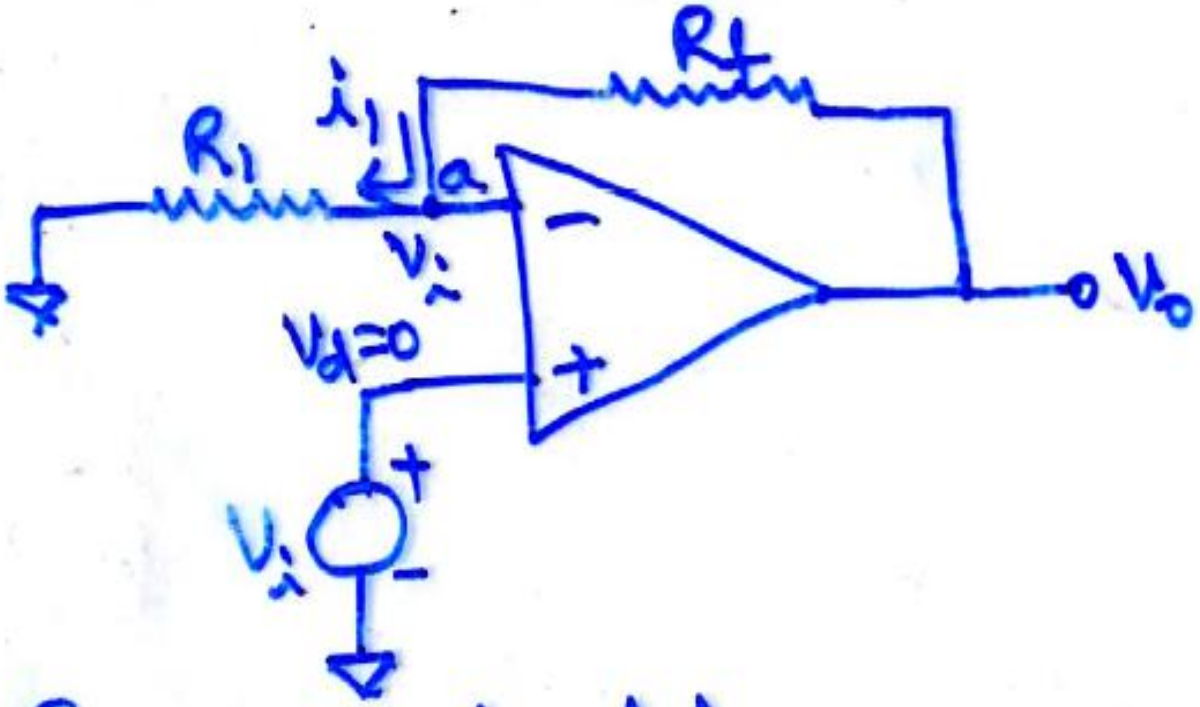


Fig 2-76 closed loop non-inverting amplifier.

Modes of Op-amp cntd..

- As Vd=0, the voltage at node ‘a’ in Figure 2.7(a) is Vi. Now R1 and Rf forms a potential divider.

  Hence Vi = (Vo/(R1+Rf)) * R1 as no current flows into op-amp.

  therefore Vo/Vi = (R1+Rf)/R1 = 1+ (Rf/R1)
- Thus, for non-inverting amplifier the voltage gain Acl = Vo/Vi = 1 + (Rf/R1)
- The gain can be adjusted to unity or more, by proper selection of resistors Rf and R1.

Modes of Op-amp cntd..

Difference Amplifier:

- Figure 4.14 shows the diagram of difference amplifier

Modes of Op-amp cntd..

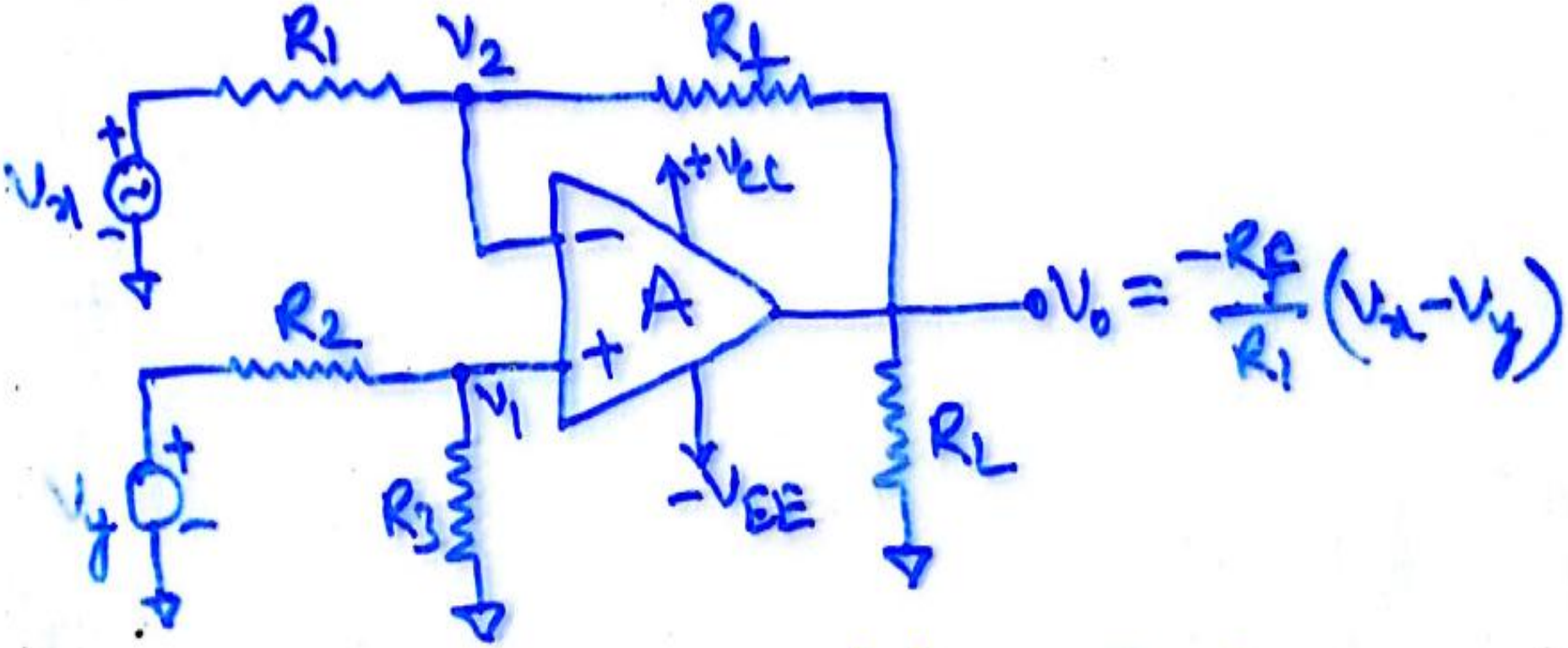


Fig 4-14 Difference amplifier. $R_1 = R_2$ & $R_f = R_3$

Modes of Op-amp cntd..

- A close examination of the figure 4-14 reveals that difference amplifier is a combination of inverting and non-inverting amplifiers i.e. when Vx = 0, circuit is a non-inverting amp.

  when Vy = 0, circuit is an inverting amp.

Voltage Gain:

- The circuit in the figure 4-14 has two inputs Vx and Vy. Therefore we use super position theorem in order to establish the relation ship between inputs and output.

Modes of Op-amp cntd..

- When Vy = 0, the output voltage due to Vx only is
  Vox = -(Rf/R1) Vx ------ eq(1)a

  Similarly when Vx=0, the configuration is a non-inverting amplifier having a voltage divider network composed of R2 and R3 at the non-inverting input. Therefore V1 = (R3/R2+R3) (Vy)

  the output due to Vy alone is

  Voy = (1 + Rf/R1) V1 ➔

  Voy= (R1+Rf)/R1 (R3/R2+R3) Vy

Since R1 = R2 and Rf = R3, Voy= (Rf/R1) (Vy) ---- eq(1)b

Modes of Op-amp cntd..

Thus from equations (1)a and (1)b, the net output voltage is $V_o = V_{ox} + V_{oy}$

➔ $V_o = (-R_f/R_1)(V_x - V_y) = -(R_f/R_1) V_{xy}$

therefore the voltage gain $A_d = V_o/V_{xy} = -R_f/R_1$

- Note that the gain of the difference amplifier is the same as that of the inverting amplifier.

Input Resistance:

The input resistance Rif of the difference amplifier is the resistance determined looking into either one of the two input terminals with the other grounded

Modes of Op-amp cntd..

- Therefore with Vy = 0, the input resistance of the inverting amplifier is **Rifx = R1** ------ eq(2)a
- Similarly with Vx=0, the input resistance of non-inverting amplifier is **Rify =R2+R3** --eq(2)b
- Therefore from eqs 2a and 2b, it is obvious that the input resistances seen by the signal sources Vx and Vy are not the same.

Modes of Op-amp cntd..

Example: In the circuit of figure 4-14, R1=R2=1KΩ, Rf=R3=10KΩ, and the op-amp is a 741C, a) what are the gain and input resistance of the amplifier?

(b) Calculate the output voltage Vo if Vx=2.7 Vpp and Vy= 3 Vpp sine waves at 100Hz.

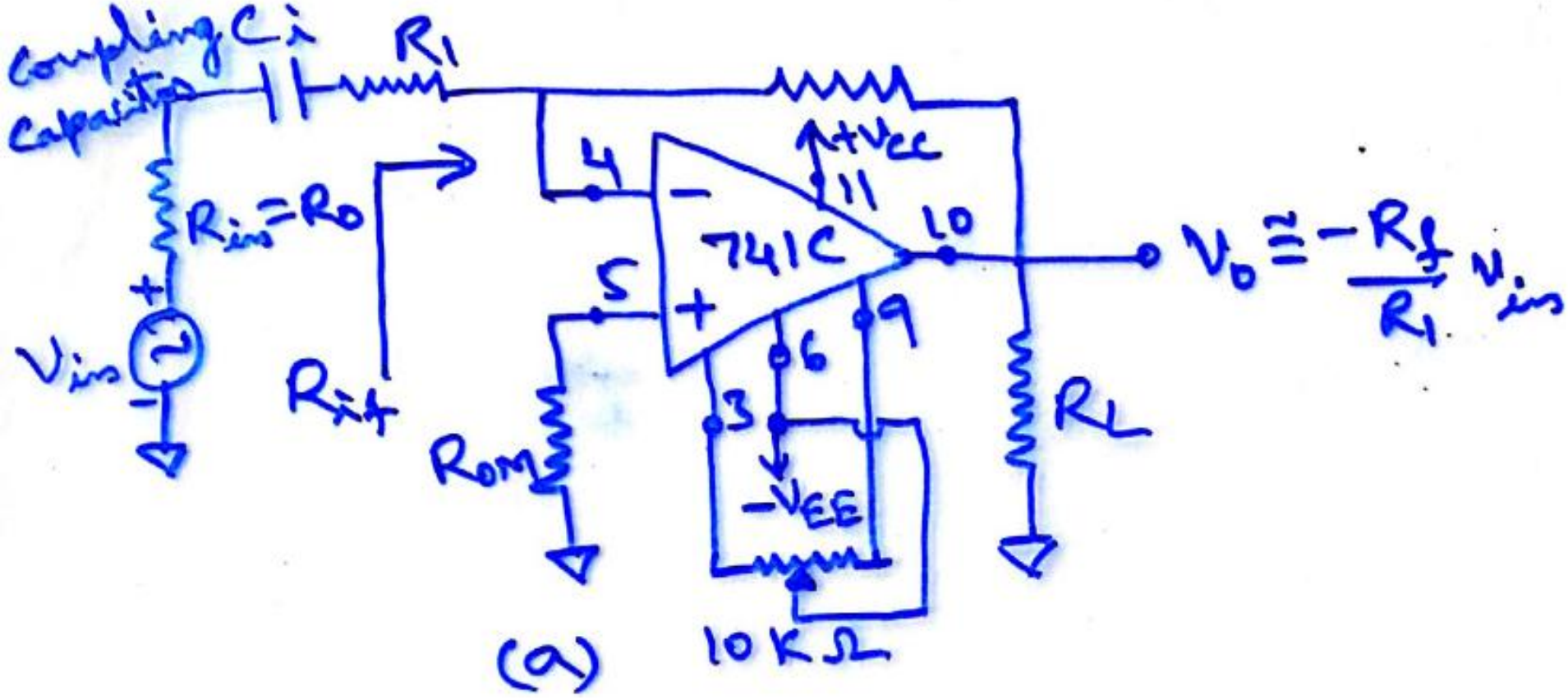
Solution: (a) Ad= -Rf/R1=-10KΩ/1KΩ = -10 Rifx = R1 = 1KΩ and Rify = R2 + R3 = 11KΩ

(b) Output voltage Vo= Ad Vxy = Ad(Vx-Vy)
= -10(2.7 – 3) = -10(-0.3) = 3 V peak to peak sine wave at 100Hz.

AC Amplifier

- If an AC input is riding on some DC level, it is necessary to use an AC amplifier with a coupling capacitor to block the DC amplification.
- For example, in an audio receiver system that consists of a number of stages, because of thermal drift, component tolerances, and variations the DC level is produced.
- To prevent the amplification of such DC levels, the coupling capacitors must be used between the stages.
- The figure 7-3 shows the AC inverting and non-inverting amplifiers with coupling capacitors.

AC Amplifier cntd..



AC Amplifier cntd..

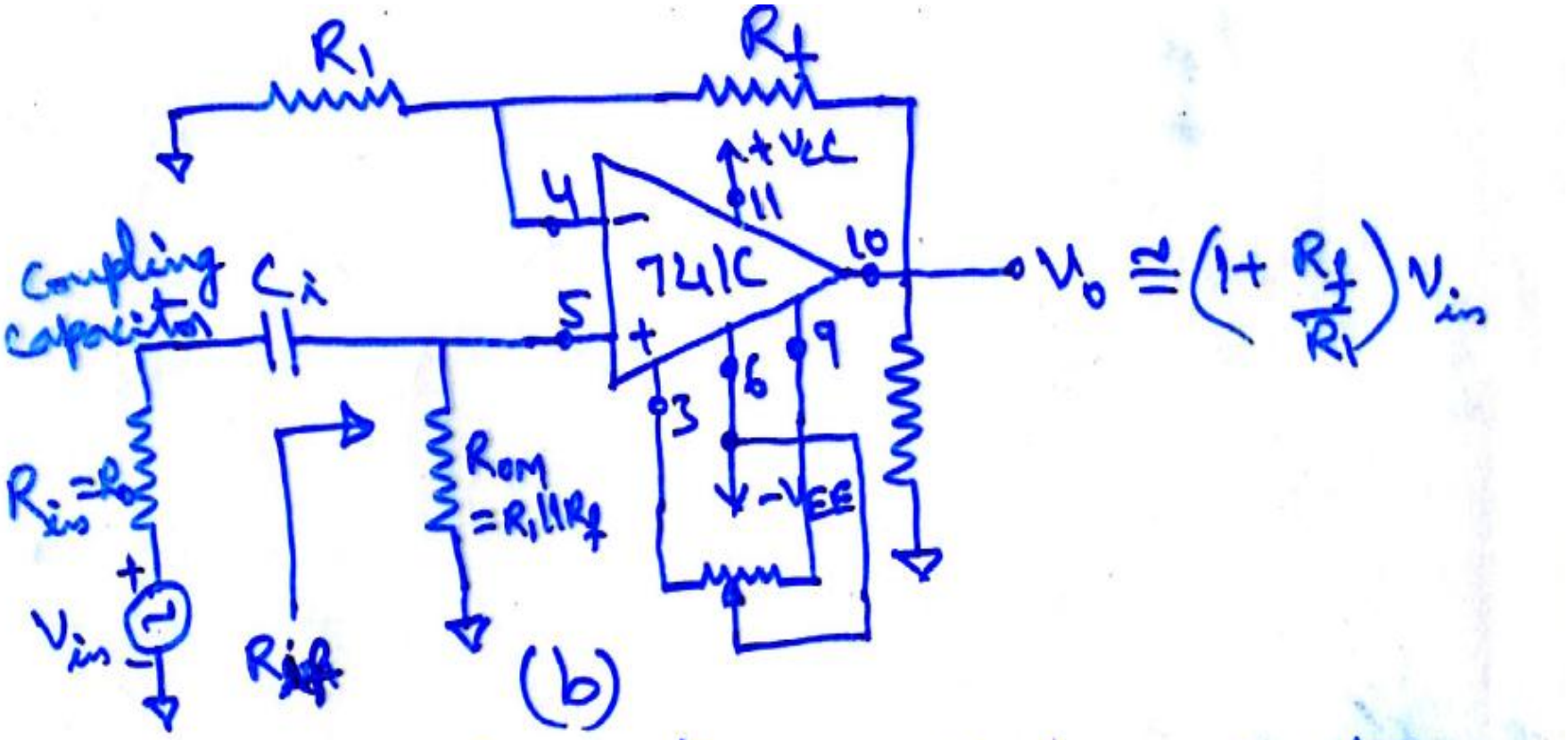


Fig 7-3 (a) Ac inverting amp. (b) Ac noninverting amp

AC Amplifier cntd..

- The coupling capacitor not only blocks the DC voltage but also set the low frequency cut off limit which is given by

$$f_L = 1/2\pi C_i(R_{if}+R_o)$$

Derivation of fL:

- The input circuit of AC inverting amplifier of Figure 7-3a is drawn in figure C-1.

AC Amplifier cntd..

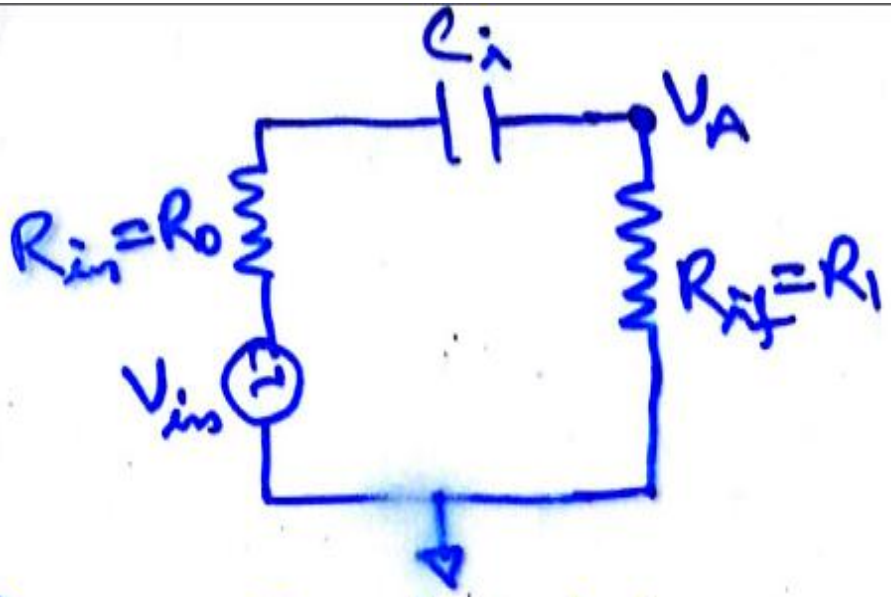


Fig C-1. Input ckt for the ac inverting amp. of fig 7-3(a)

AC Amplifier cntd..

- The voltage VA is amplified by the AC inverting amplifier, hence it is necessary to determine VA as a function of input voltage Vin
- Using voltage divider rule, we get

$$VA = Rif\ Vin/(Ro + 1/jwCi + Rif) \quad \text{-------- eq(1)}$$

where Rif – input resistance of inverting amplifier

Ro – Source resistance, Rin

Rearranging eq (1)

$$VA = j\ (Rif\ w\ Ci)\ Vin/j(Rif + Ro)\ w\ Ci + 1$$

$$= j\ (2\pi f\ Ci\ Rif)\ (Vin)\ /\ j\ ((2\pi f\ Ci)(Rif+Ro) + 1)$$

AC Amplifier cntd..

- $VA = j(2\pi f\ Ci\ Rif)\ (Vin)/(j(f/fL)+1)$

  where f – Input frequency (Hz)

  $fL = 1/2\pi\ Ci(Rif + Ro)$

  where fL = low frequency cut-off or low end of bandwidth

  Ci= DC blocking capacitor

  Rif = AC input resistance of second stage

  Ro = AC output resistance of 1^{st} stage or Rin

AC Amplifier cntd..

- The high end of the bandwidth is given by

  fH = UGB (K)/ |Acl|

  where UGB – Unity gain bandwidth = 10^6

  K = 0.909 = Constant factor

  Acl = closed loop gain

Therefore bandwidth of the amplifier is

  BW = fH – fL

- The Resistor Rom is used to minimize the effect of output offset voltage
- Since the reactance of Ci is negligible with in the bandwidth, the closed loop gain of the AC inverting amplifier is **Acl = -Rf/R1**
- And the closed loop gain of the AC non-inverting amplifier is

  Acl = 1 + Rf/R1

AC Amplifier cntd..

Example : in the circuit of Fig 7.3(a) Rin=50Ω, Ci= 0.1 μF, R1=100 Ω, Rf= 1 KΩ, Rl=10KΩ and supply voltages=+ or – 15 V. Determine the bandwidth of the amplifier

AC Amplifier cntd..

Solution: Band width = fH – fL

where fH = (UGB) (K)/|Acl|

Acl = -Rf/R1 = - 1KΩ / 100 Ω = -10

therefore fH = 10^6(0.909)/10 = 90.9 KHz and

fL= 1/2πCi(Rif+Ro)

where Rif = input resistance of the inverting amplifier with feedback

Rif=R1=100Ω

Ro= Source resistance = Rin = 50 Ω

therefore fL= 1/2π (10^-7) (100+50) = 10.6 KHz

Therefore bandwidth = 90.9 KHz – 10.6 KHz = 80.3 KHz

Differentiator

Differentiator:

- A differentiator is a circuit in which the output waveform is the derivative of input waveform. A differentiator circuit is shown in the figure 4.21(a).

Differentiator cntd..

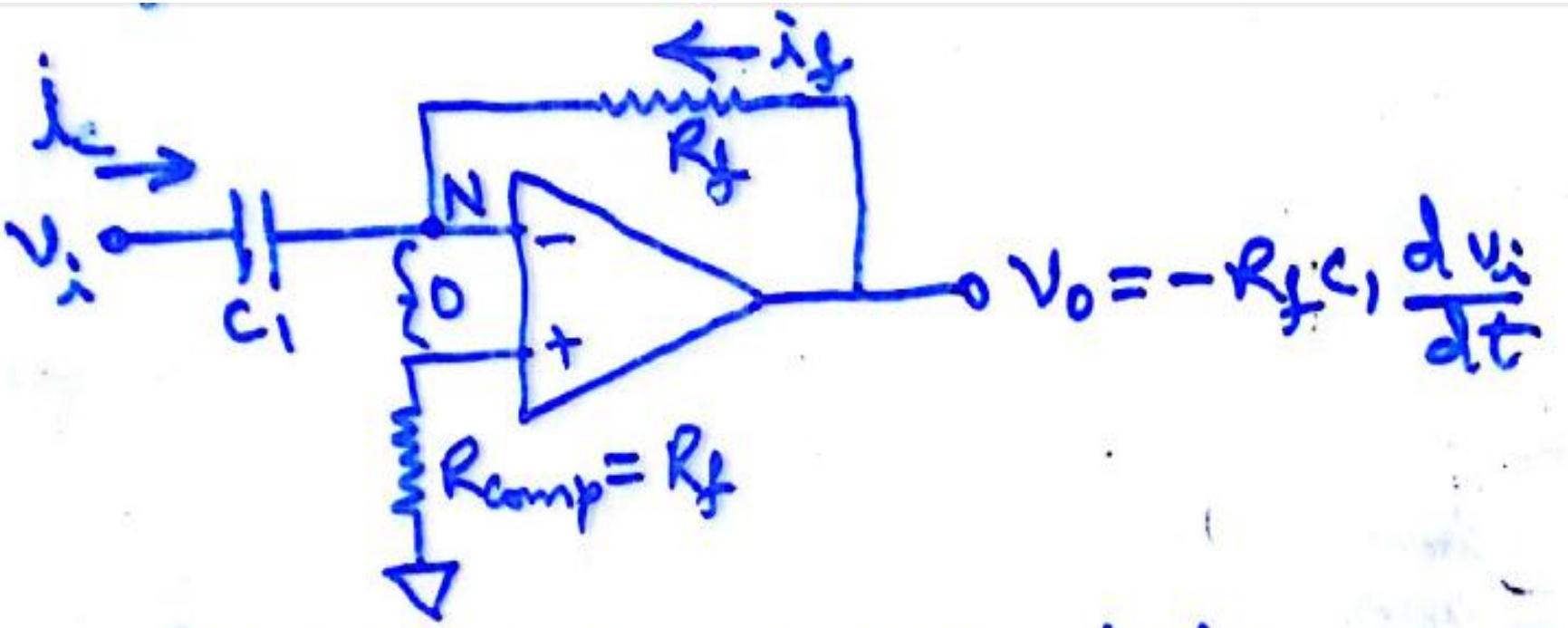


Fig 4.21(a) op-amp differentiator

Differentiator cntd..

Analysis:

- The node N is at virtual ground potential ie Vn=0. The current ic through the capacitor is ic= C1 d(Vi-Vn)/dt = C1 dVi/dt
- The current If(not the English word if) through the feedback resistor = Vo/Rf and there is no current into the op-amp

Therefore nodal equation at node N is

$$C1\ dVi/dt + Vo/Rf = 0$$

$$\Longrightarrow\ Vo = -Rf\ C1\ dVi/dt \quad \text{------ eq(1)}$$

- The minus sign indicates a 180° phase shift of the output waveform Vo with respect to the input signal.

Differentiator cntd..

- The phasor equivalent of equation (1). is

  Vo(s) = - Rf C1 S Vi(s) where Vo & Vi are the phasor representation of vo & vi.

In steady state put s=jw. Now the magnitude of gain A of the differentiator is

$|A| = |Vo/Vi| = |-jw\ Rf\ C1| = w\ Rf\ C1$ ---- eq(2)

Eq (2) may be written as

$|A| = f/fa$ where $fa = 1/2\pi\ Rf\ C1$

At f = fa, |A| = 1 ie = 0 dB, and the gain increases at a rate of +20dB/decade.

Thus at high frequency, a differentiator may become unstable and break into oscillations .

Differentiator cntd..

- There is one more problem in the Differentiator of figure 4.21(a).
- The input impedance (ie 1/wC1) decreases with increase in frequency there by making the circuit sensitive to high frequency noise.

Practical Differentiator:

- A practical differentiator of the type shown in Figure 4.21b eliminates the problem of stability and high frequency noise.

Differentiator cntd..

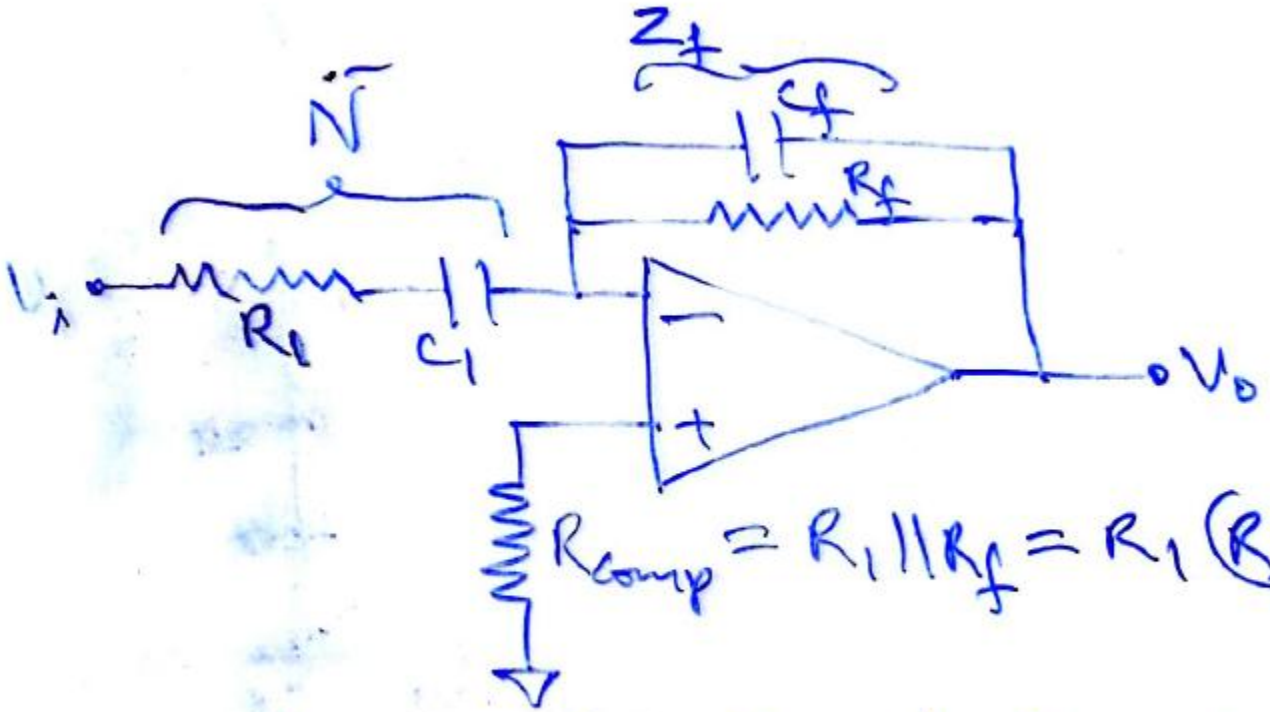


Fig 4.21(b) Practical Differentiator

Differentiator cntd..

The transfer function for the circuit in Figure 4.21b is mentioned as

$V_o(s)/V_i(s) = -Z_f/Z_i = -sR_fC_1/(1+ sR_fC_f)(1+sR_1C_1)$

For $R_fC_f = R_1C_1$, we get

$V_o(s)/V_i(s) = -sR_fC_1/(1+sR_1C_1)^2$

$= -sR_fC_1/(1+jf/fb)^2$ ----- eq(3)

where $fb = 1/2\pi R_1C_1$

from eq(3), it is evident that the gain increases at + 20 dB/decade for frequency f < fb and decreases at -20 dB/decade for f > fb as shown by dashed lines in figure 4.21(c)

Differentiator cntd..

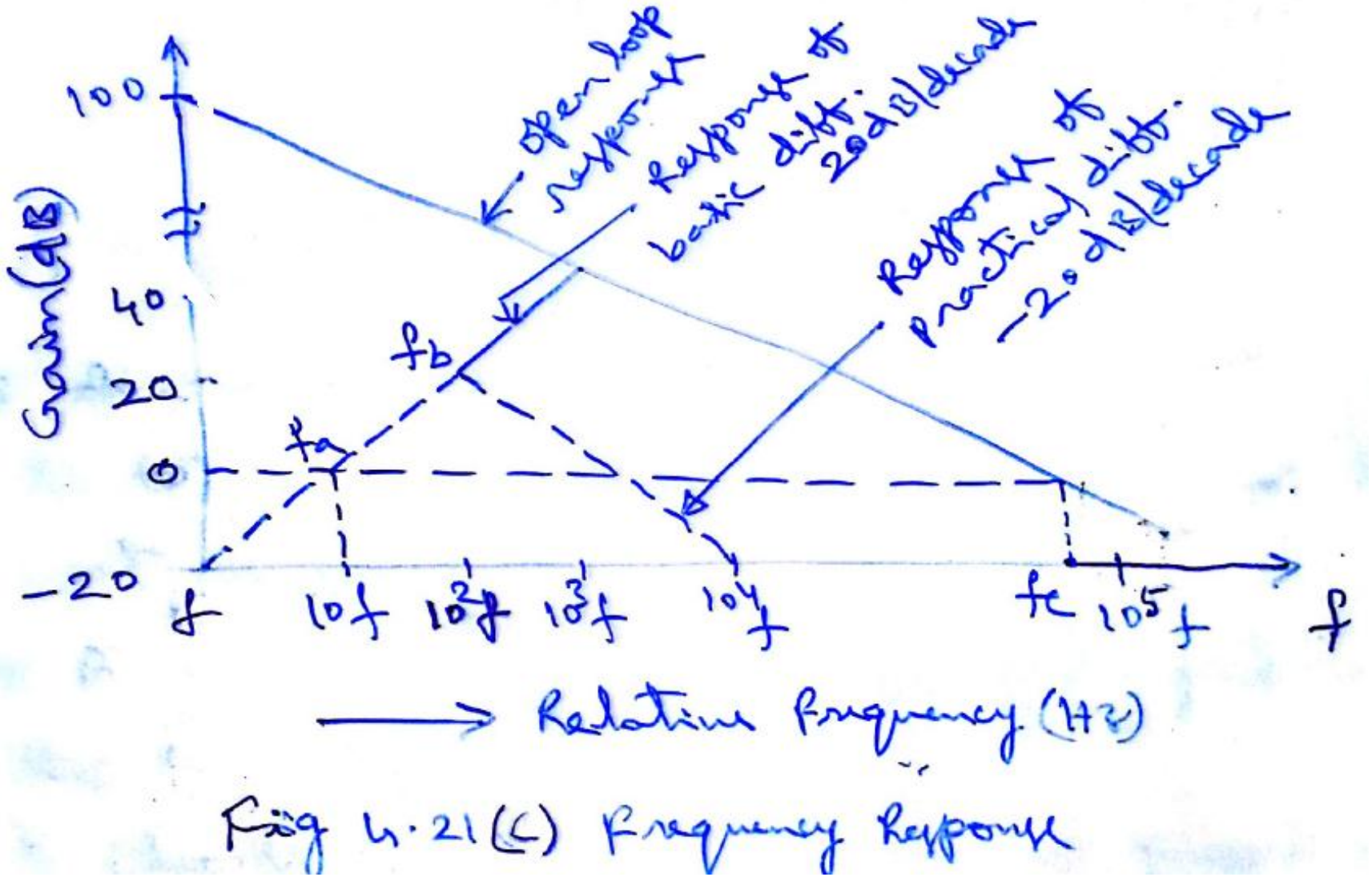


Fig 4.21(c) Frequency Response

Differentiator cntd..

- This 40 dB/decade change in gain is caused by R1C1 and RfCf factors.
- For the basic differentiator of Fig.4.21(a) the frequency response would have increased continuously at the rate of +20dB/decade even beyond fb causing stability problem at high frequency.
- Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems.
- The value of fb should be selected such that

$$fa < fb < fc$$

where fc is the unity bandwidth of the op-amp in open loop configuration.

Differentiator cntd..

- A resistance Rcomp is normally connected to the (+) input terminal to compensate for the input bias current.

A good differentiator may be designed as per the following steps.

1. Choose fa equal to the highest frequency of the input signal. Assume a practical value of C1 (< 1 μF) and then calculate Rf $f_a = 1/2\pi R_f C_1$
2. Choose fb = 10 fa (say). Now calculate the value of R1 from $f_b = 1/2\pi R_1 C_1$ and Cf so that

$$R_1C_1 = R_fC_f$$

Differentiator cntd..

Example: (a) Design an op-amp differentiator that will differentiate an input signal with fmax = 100 Hz.

(b) Draw the output waveform for a sine wave of 1V peak at 100 Hz applied to the differentiator

(c) Repeat part (b) for a square wave input.

Differentiator cntd..

- **Solution:**

a) Select fa = fmax = 100 Hz = 1/2π Rf C1

let C1 = 0.1 μF

Then Rf = 1/2π(10^2)(10^-7) = 15.9 KΩ

Now choose fb = 10 fa = 10 (100 Hz) = 1 KHz

= 1/2π R1 C1

Therefore R1 = 1/2π (10^3)(10^-7) = 1.59 KΩ

since Rf Cf = R1 C1

We get Cf =1.59 (10^3) (10^-7)/15.9(10^3) = 0.01μF

Differentiator cntd..

(b) $V_i = 1 \sin 2\pi (100) t$

from eq (1), $V_o = -R_f C_1 \frac{dV_i}{dt}$

$V_o = -(15.9\ K\Omega)(0.1\ \mu F) \frac{d[1 \sin 2\pi (10^2) t]}{dt}$

$= -(15.9\ K\Omega)(0.1\ \mu F)\, 2\pi (10^2) \cos[2\pi(100)t]$

$= -0.999 \cos[2\pi (100) t]$

$= -1 \cos[2\pi (100) t]$

The input and output waveforms are shown in Figure 4.22

Differentiator cntd..

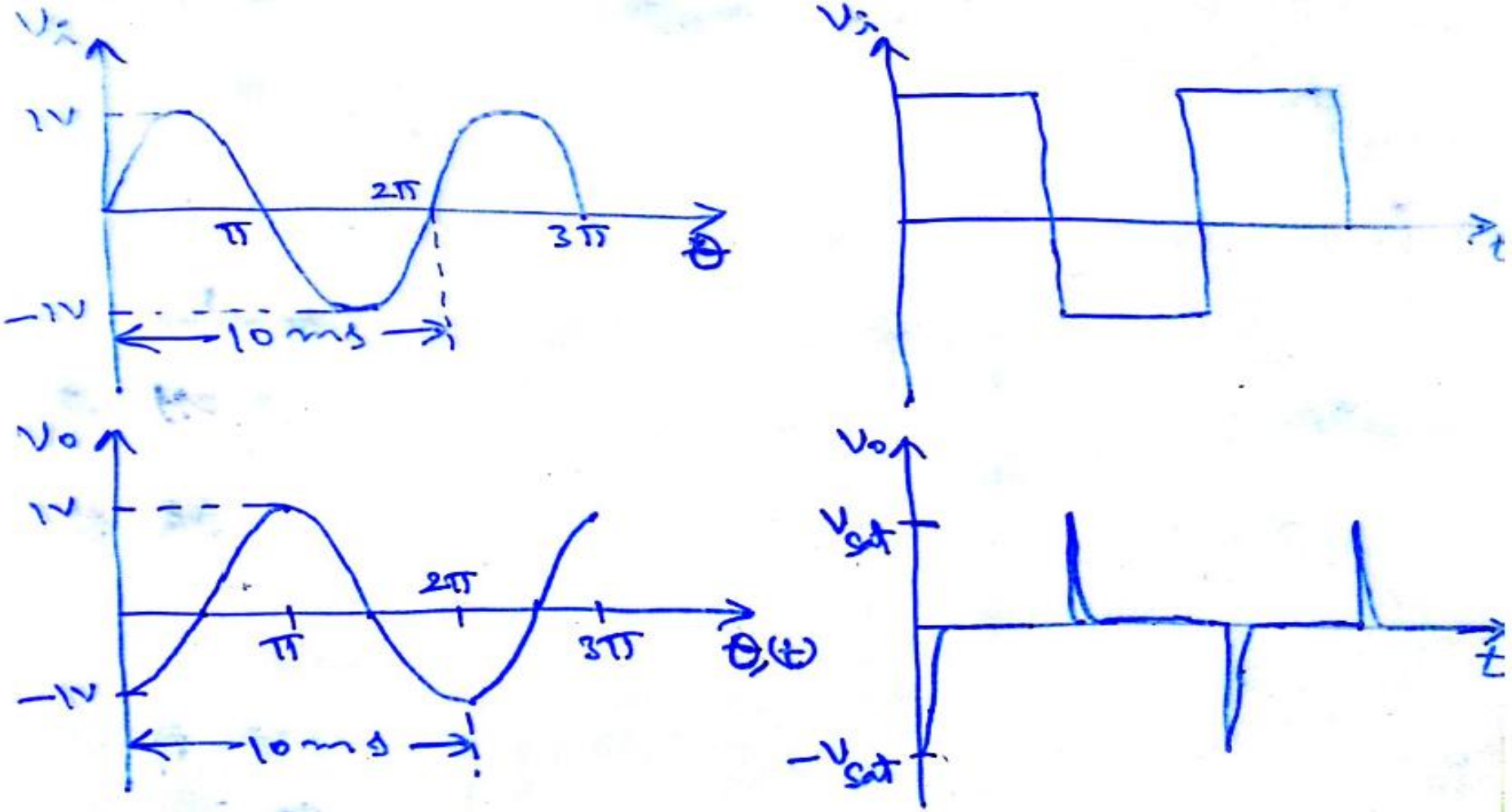


Fig 4.22(a) Sine-wave input & Cosine output
(b) Square wave input & Spike output.

Integrator

- By interchanging the resistor and capacitor of the Differentiator, we get the circuit of an integrator which is shown in the figure 4.23(a).

Integrator cntd..

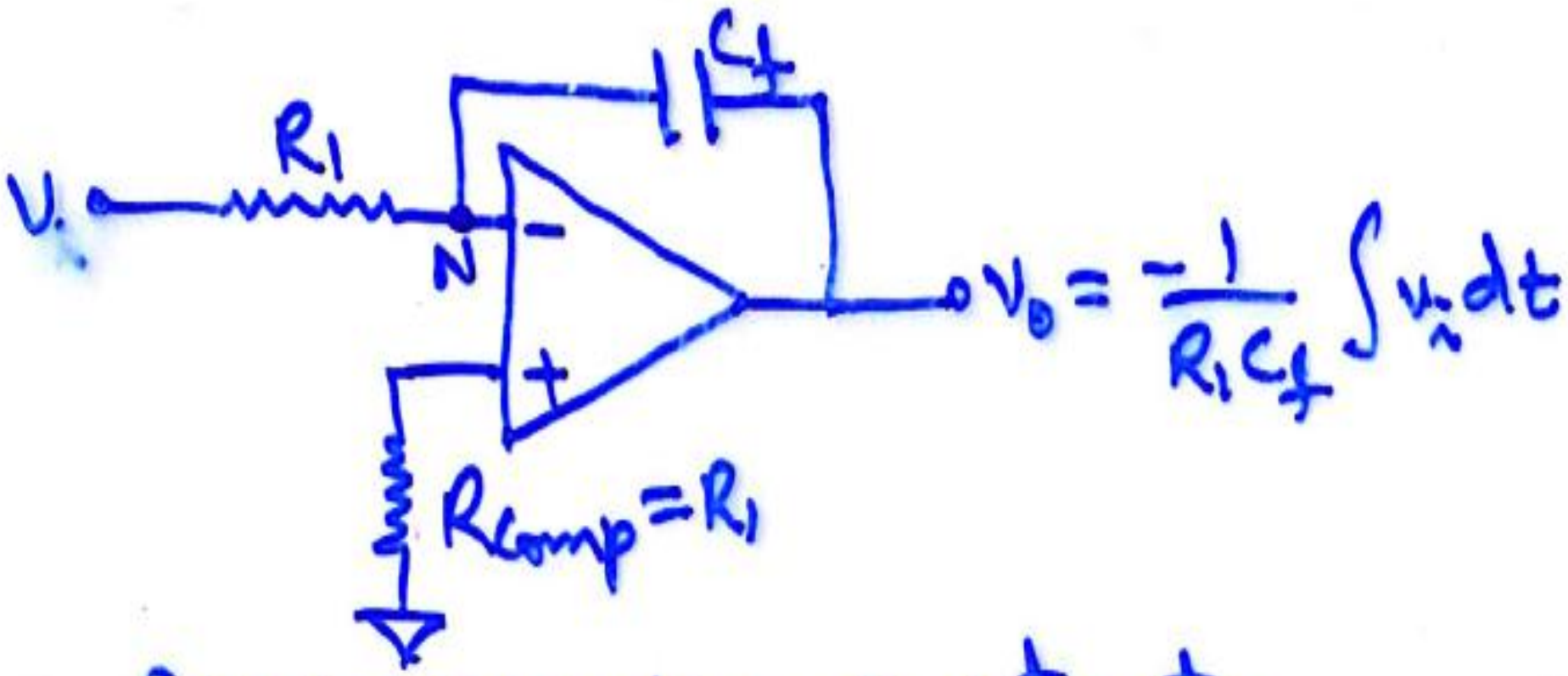


Fig 4.23(a) op-amp integrator

Integrator cntd..

- The nodal equation at node N is

  $(Vi/R1) + Cf\ dVo/dt = 0$

  ➔ $dVo/dt = -(1/R1\ Cf)\ Vi$

  ➔ ${}_0\int^t dVo = (-1/R1Cf)\ {}_0\int^t Vidt$

  $Vo(t) = (-1/R1Cf)\ {}_0\int^t Vi(t)dt + Vo(0)$ ----- eq(1)

  where Vo(0) is the initial o/p voltage.
- Here R1Cf is the time constant of the integrator

Integrator cntd..

- Here –ve sign is present, hence it is called inverting integrator.
- Rcomp is the resistor to minimize the effect of input bias current.
- The operation of the integrator can also be studied in the frequency domain. In phasor notation the equation (1) can be written as

$$V_o(s) = -(1/sR_1C_f)\, V_i(s)$$

In steady state, put s=jw and we get

$$V_o(jw) = -(1/jwR_1C_f)\, V_i(jw)$$

Integrator cntd..

- So the magnitude of the gain is

$$|A| = |Vo(jw)/Vi(jw)| = |-1/jwR1Cf|$$

$$= 1/wR1Cf = 1/(f/fb)$$

Where $fb = 1/2\pi R1Cf$

- The frequency response is shown in the figure 4.23b

Integrator cntd..

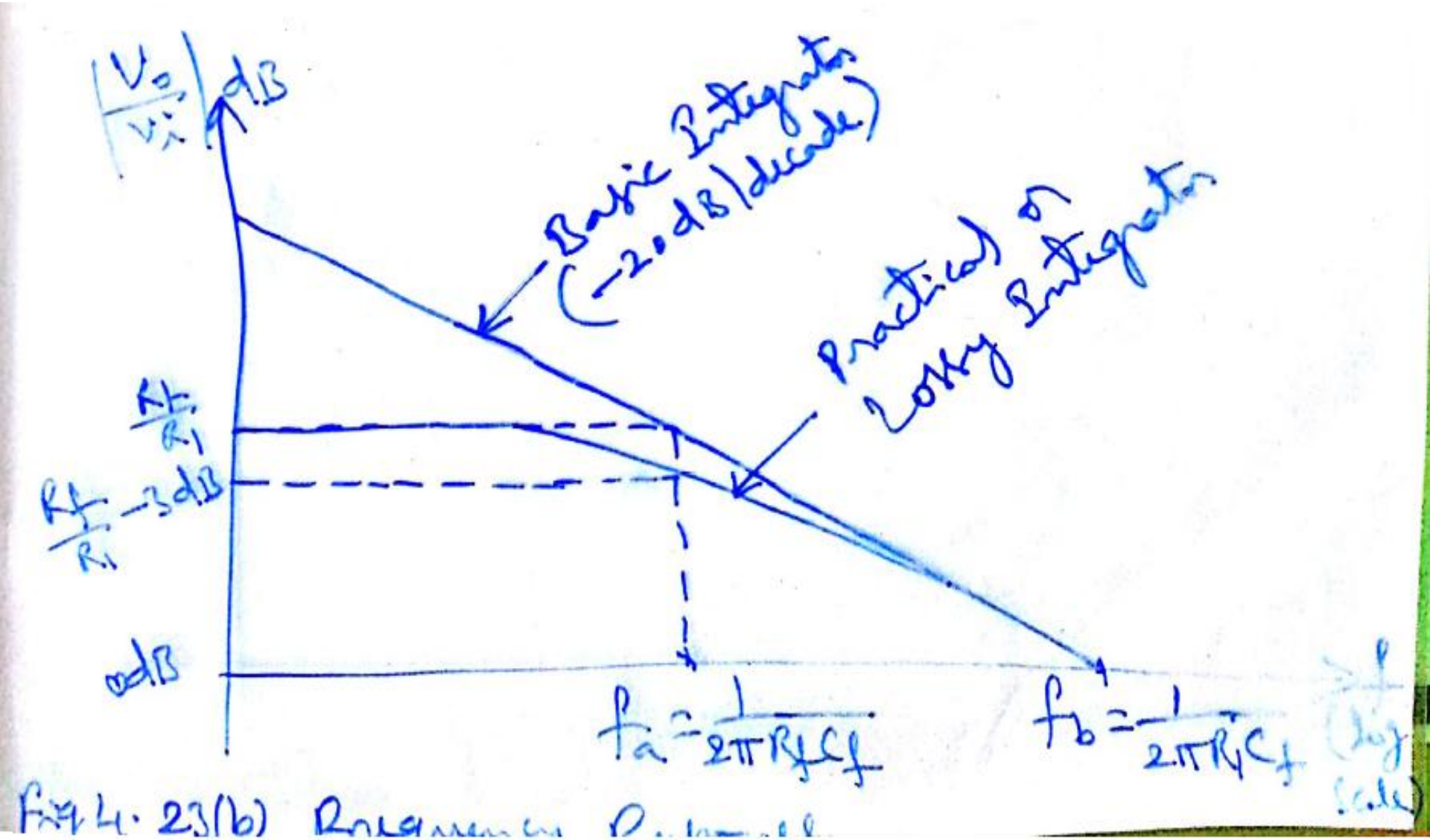


Fig 4.23(b) Frequency Response

Integrator cntd..

- The Bode plot of basic integrator is a straight line of slope -20 dB/decade.
- The frequency fb is the frequency at which the gain of the integrator is 0 dB and is given by

$$fb = 1/2\Pi R1Cf$$

- As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in the differentiator. However, at low frequencies such as DC (w=0), the gain becomes infinite (ie saturates). The solution to this problem is a practical integrator circuit.

Integrator cntd..

Practical Integrator Circuit (Lossy Integrator):

- The gain of an integrator at low frequency (DC) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance Rf as shown in the Figure 4.23c

Integrator cntd..

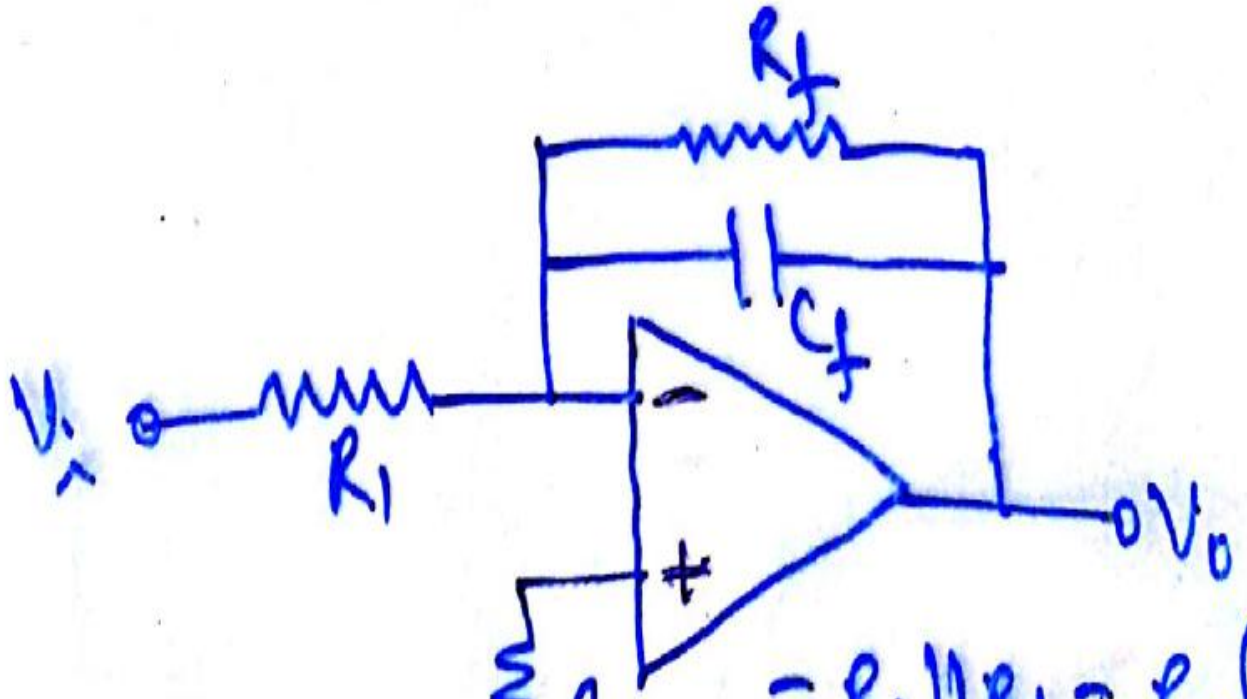


Fig 4.23(c) practical or Lossy Integrator Circuit

Integrator cntd..

- The parallel combination of Rf and Cf behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called as a Lossy integrator.
- The resistor Rf limits the low frequency gain to –Rf/R1 (generally Rf = 10 R1) and thus provides DC stabilization.

Integrator cntd..

Analysis:

- The nodal equation at the inverting input terminal of the op-amp is

  $V_i(s)/R1 + sCf\, V_o(s) + V_o(s)/Rf = 0$

From which we have

$$V_o(s) = -\left(1/(sR1Cf + R1/Rf)\right) V_i(s)$$

- If Rf is large, the lossy integrator approximates the ideal integrator.
- For S=jw, the magnitude of the gain of Lossy integrator is given by

$$|A| = |V_o/V_i| = 1/(\sqrt{w2R1^2\, Cf^2 + R1^2/Rf^2})$$

$$= Rf/R1/(\sqrt{(1+(wRf\, Cf)^2}) \quad \text{------ eq(2)}$$

Integrator cntd..

- The Bode plot of the Lossy Integrator is also shown in the Figure 4.23b. At low frequencies the gain is constant at Rf/R1.
- The break frequency (f = fa) at which the gain is 0.707 (Rf/R1) is calculated from eq (2) as

  $\sqrt{}$(1+ w Rf Cf)^2 = $\sqrt{}$2

  ➔ wRf Cf = 1 ➔ f = 1/2πRf Cf

  solving for f = fa, we get fa = 1/2 πRf Cf
- This frequency tells us where the useful integration range starts in Figure 4.23b

Integrator cntd..

- If the input frequency is lower than fa, the circuit acts like a simple inverting amplifier and no integration results.
- At the input frequency equal to fa, 50% accuracy results.
- The practical thumb rule is that if the input frequency 10 times fa, then 99% accuracy can result.

Comparator

- A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.
- There are basically two types of comparators.

1. Non-inverting comparator
2. Inverting comparator

Comparator cntd..

Non-Inverting Comparator:

- The circuit of figure 5.2a is called a non-inverting comparator.
- A fixed reference voltage Vref is applied to – input and a time varying signal Vi is applied to +input.
- There are 3 conditions for a comparator. They are
  Vi < Vref → Vo = -Vsat

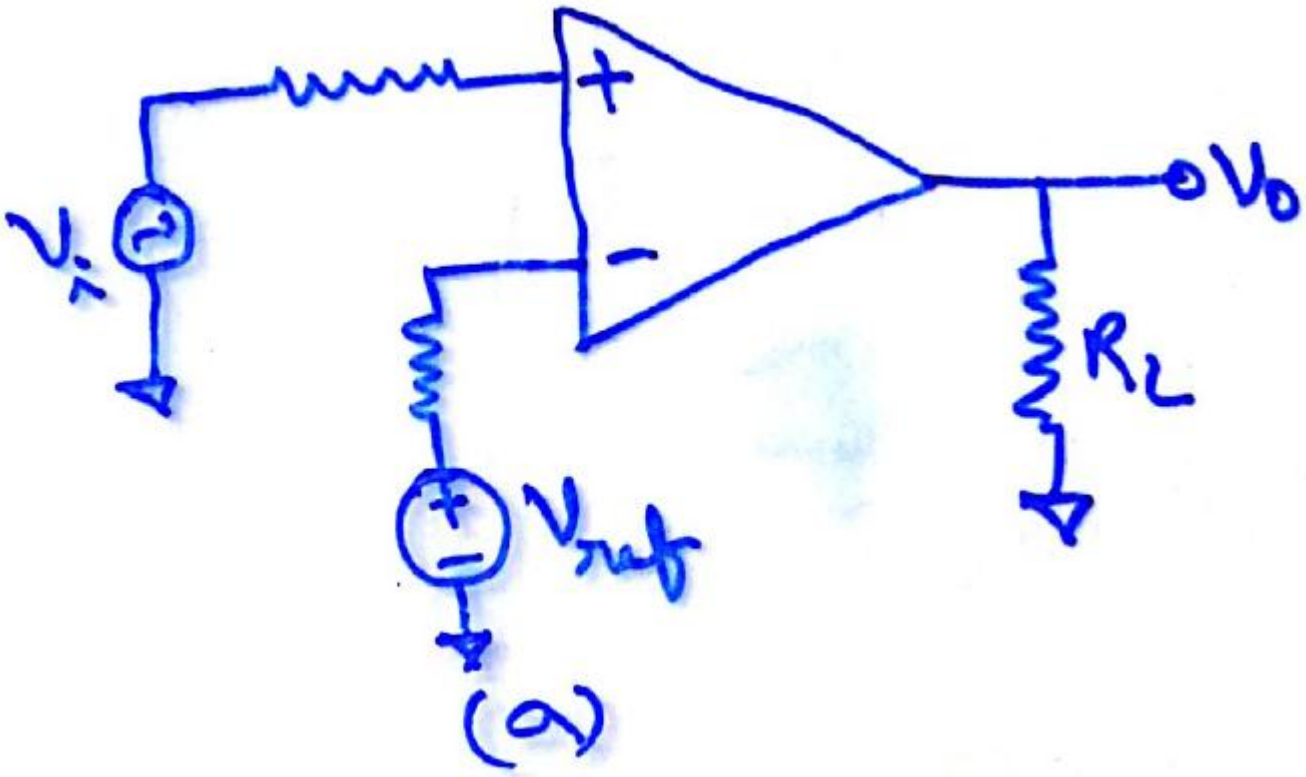
  Vi > Vref → Vo = +Vsat

  Vi = Vref → changes the state of op-amp

Comparator cntd..

- The output waveform for a sinusoidal input signal applied to the +ve input is shown in figure 5.2 (b) and (c) for +ve and –ve Vref respectively.

Comparator cntd..



Comparator cntd..

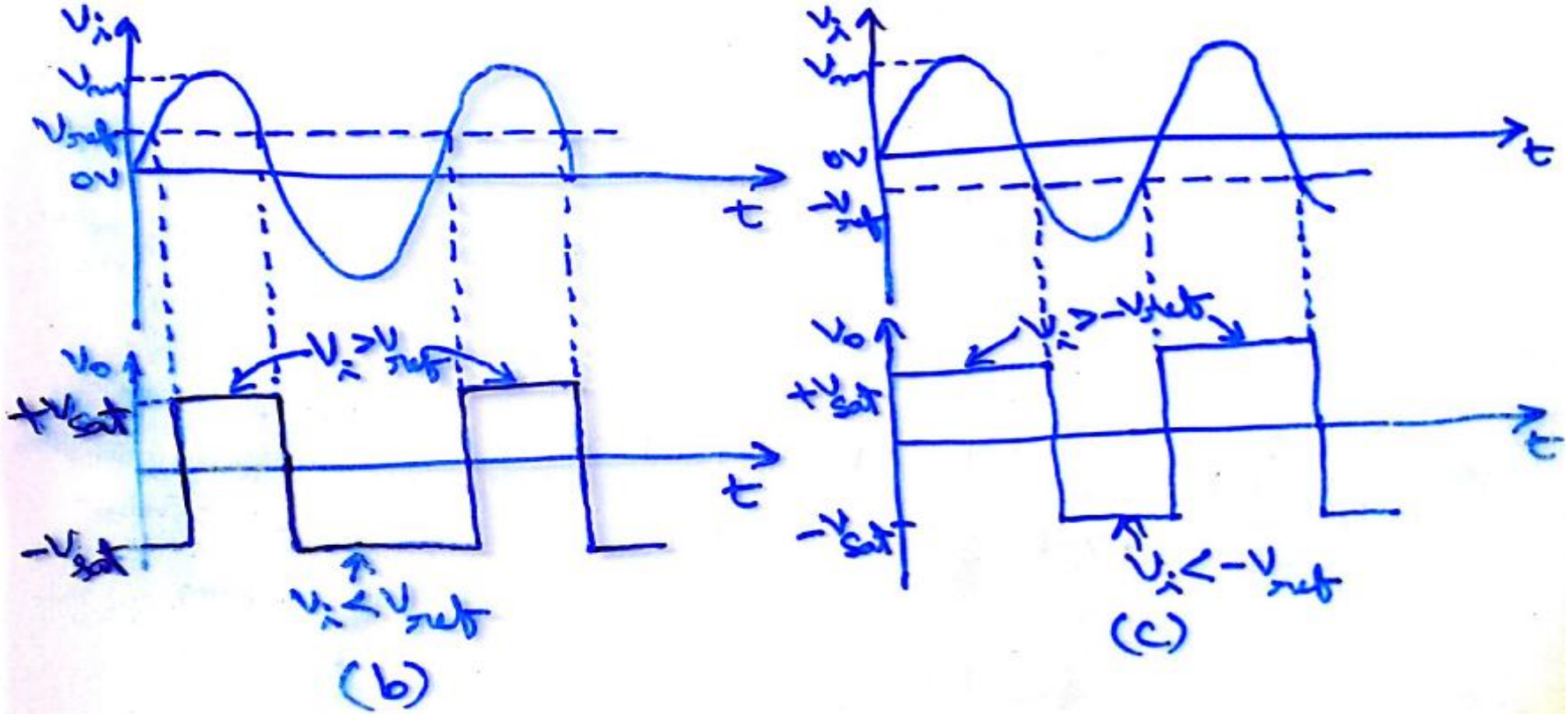


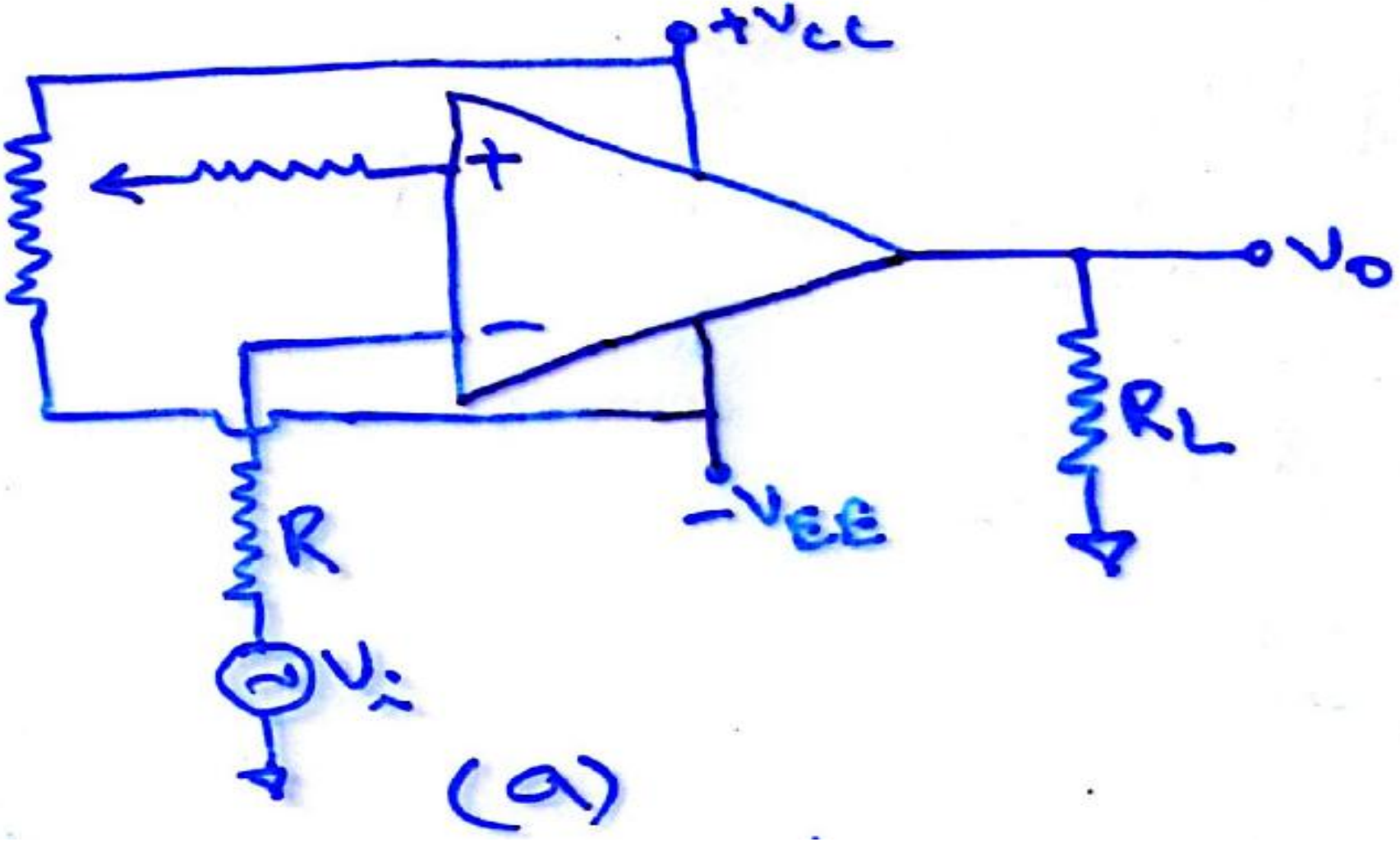
Fig 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} +ve (c) V_{ref} -ve

Comparator cntd..

Inverting Comparator:

- Figure 5.3(a) shows a practical inverting comparator in which the reference voltage Vref is applied to the +input and Vi is applied to the –ve input.
- For a sinusoidal input signal, the output waveform is shown in in figure 5.3(b) and 5.3(c) for Vref +ve and –ve respectively.

Comparator cntd..



Comparator cntd..

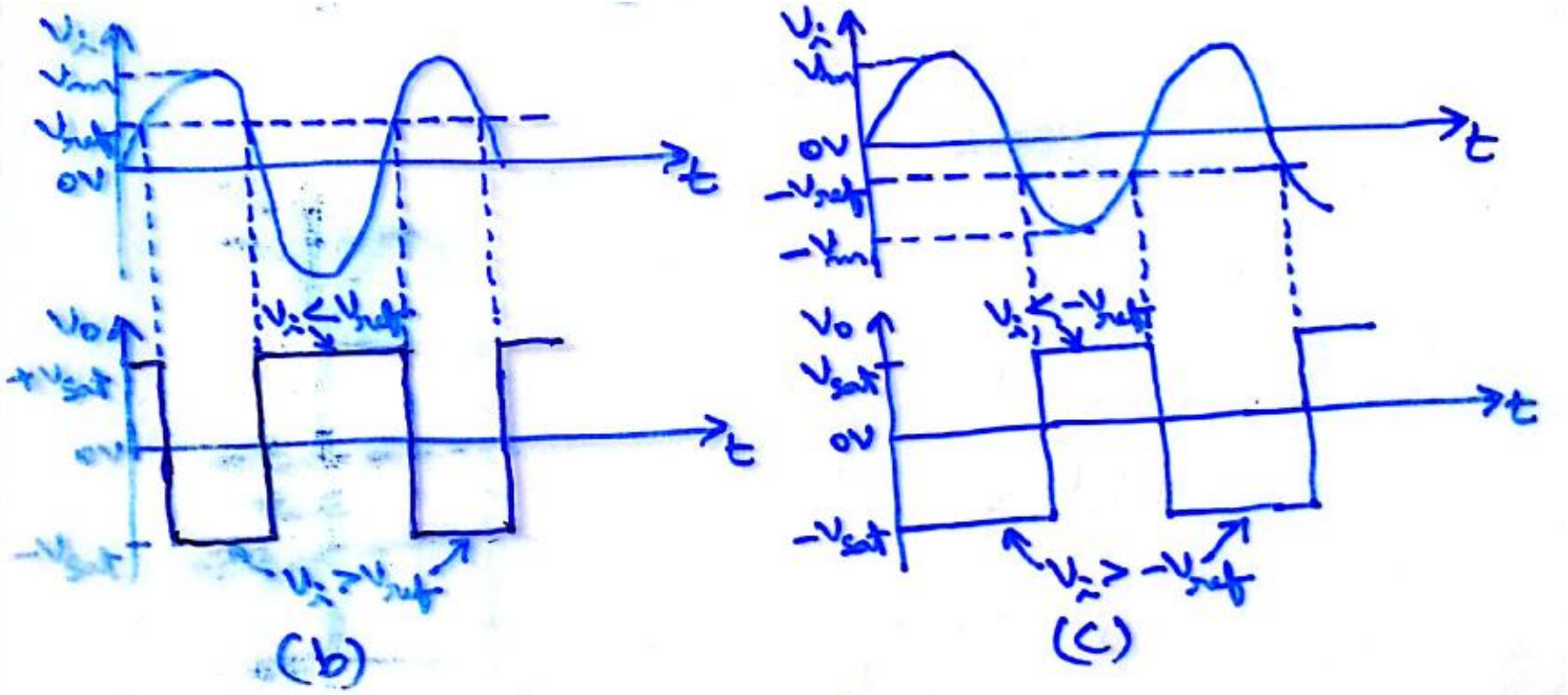
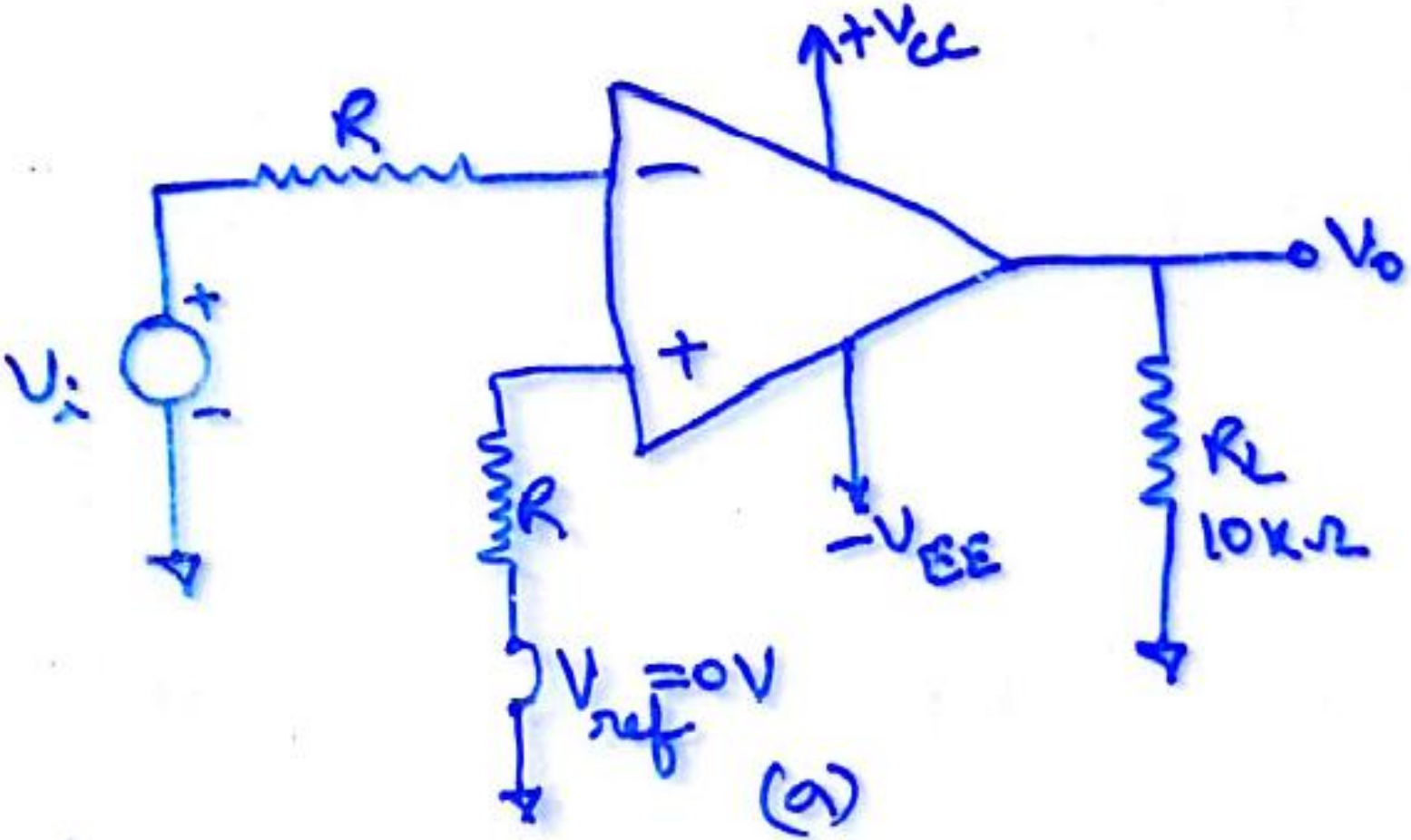


Fig 5-3(a) Inverting Comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$

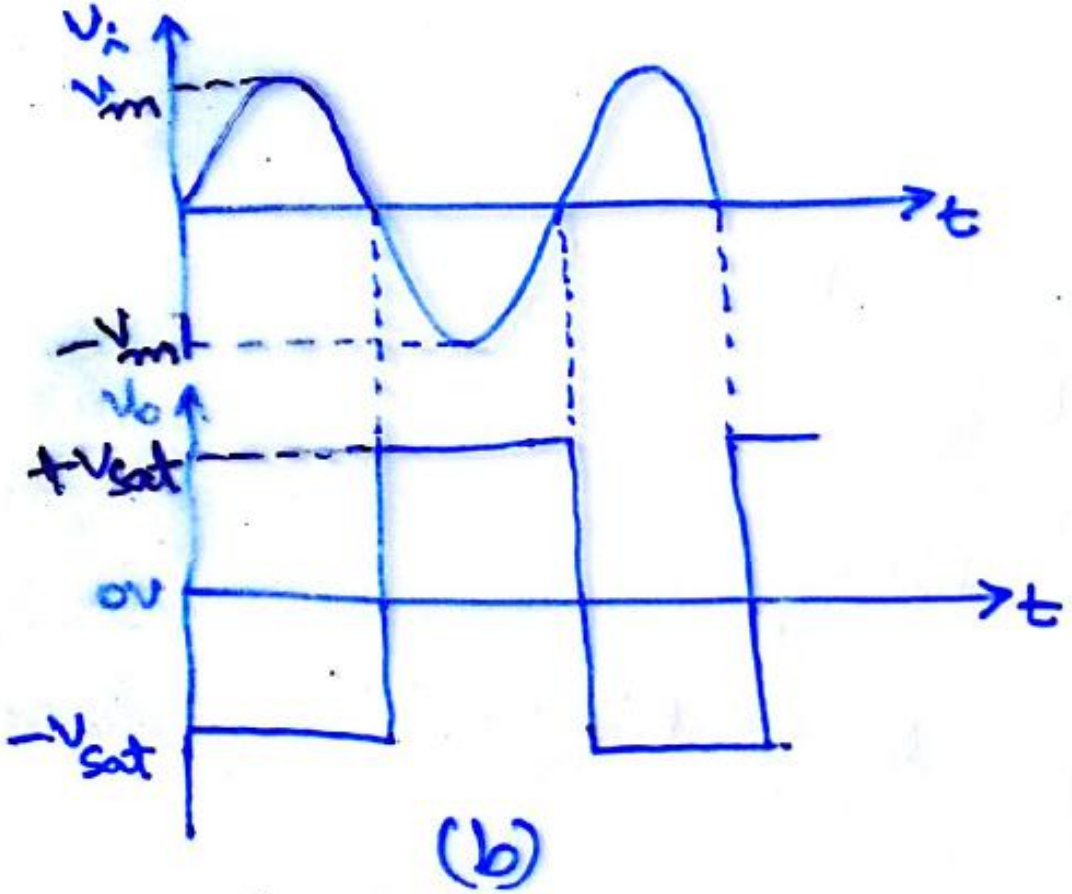
Applications of Comparator

- Some important applications of comparator are
  - Zero crossing detector
  - Window detector
  - Time marker generator
  - Phase meter.

Zero crossing detector



Zero crossing detector cntd..



(b)

Fig 5.4 (a) Zero crossing detector (b) Input and o/p waveforms

Zero crossing detector cntd..

- The basic comparators either non-inverting or inverting can be used as a zero crossing detector provided that Vref is set to zero. An inverting zero-crossing detector is shown in figure 5.4 (a).
- The input and output waveforms are shown in Figure 5.4 (b).
- The circuit is also called as a sine to square wave generator.

Regenerative comparator (Schmitt trigger)

- If positive feedback is added to the comparator circuit, gain can be increased greatly.
- Figure 5.8 (a) shows a regenerative comparator. The circuit is also known as Schmitt trigger

Regenerative comparator (Schmitt trigger) cntd..

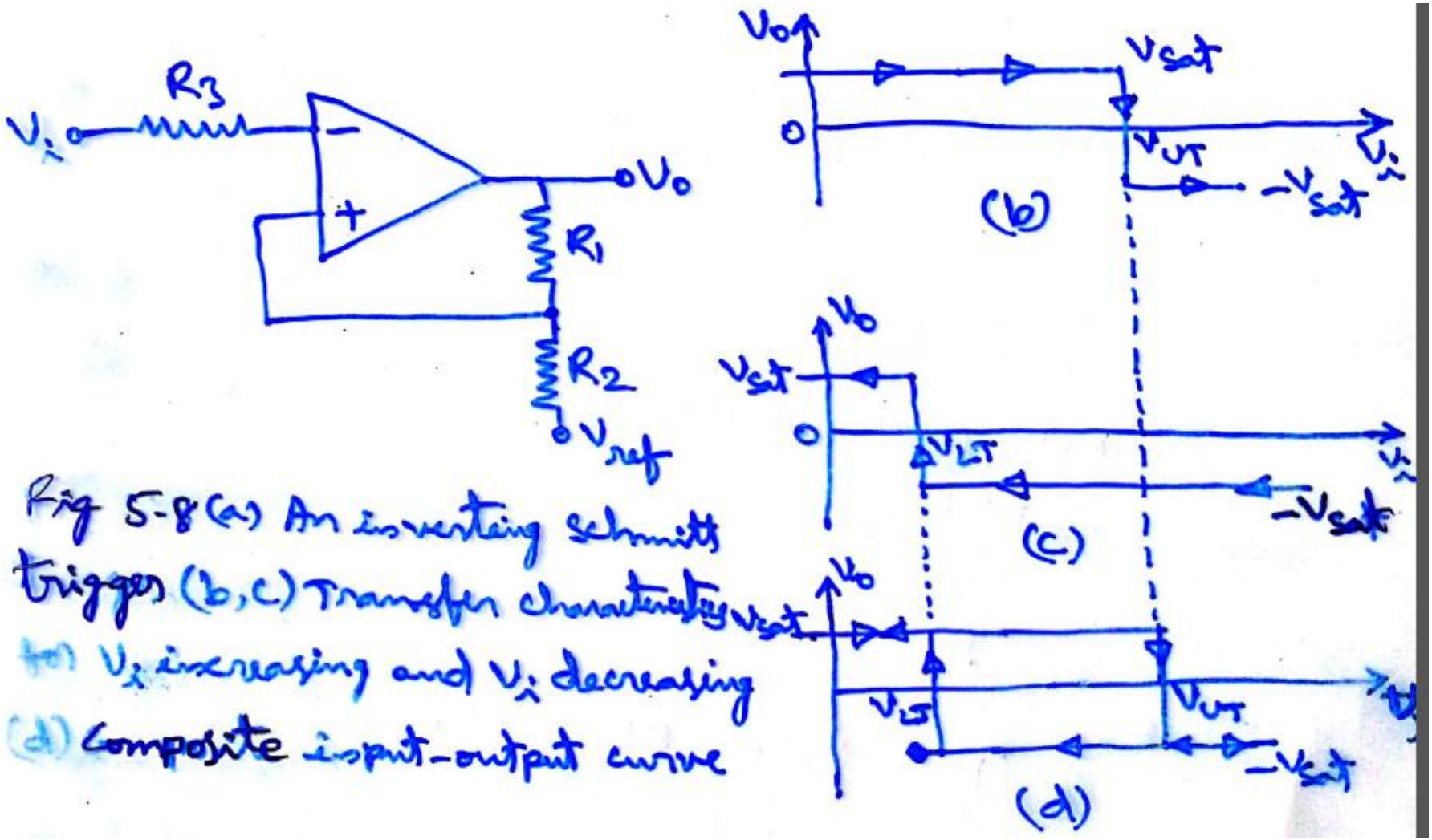


Fig 5-8 (a) An inverting schmitt trigger (b,c) Transfer characteristics for V_i increasing and V_i decreasing (d) Composite input-output curve

Regenerative comparator (Schmitt trigger) cntd..

- The input voltage Vi triggers the output Vo every time it crosses certain voltage levels. These voltage levels are called Upper threshold voltage (Vut) and Lower threshold voltage (Vlt).
- The hysteresis width is the difference between these two threshold voltages ie Vut – Vlt. These threshold voltages are calculated as follows.
- Suppose that the output voltage Vo is +Vsat. The voltage at +ve input terminal will be

  $V_{ref} + (R2/(R1+R2))\,(V_{sat} - V_{ref}) = V_{ut}$

Regenerative comparator (Schmitt trigger) cntd..

- This voltage is called as Upper threshold voltage Vut
- As long as Vi is less than Vut, the output Vo remains constant at +Vsat. When Vi is just greater than Vut, the output regeneratively switches to – Vsat and remains at this level as long as Vi > Vut as shown in Figure 5.8 (b).
- For Vo = -Vsat, the voltage at +ve input terminal is

  $V_{ref} + (R2/R1+R2)(-V_{sat} - V_{ref}) = V_{lt}$

  $V_{ref} - (R2/R1+R2)(V_{sat} + V_{ref}) = V_{lt}$

this voltage is referred to as lower threshold voltage Vlt

Regenerative comparator (Schmitt trigger) cntd..

- The input voltage Vi must become lesser than Vlt in order to cause Vo to switch from –Vsat to +Vsat. A regenerative transition takes place as shown in Figure 5.8(c) and the output Vo returns from –Vsat to +Vsat almost instantaneously.
- The complete transfer characteristics are shown in Figure 5.8 (d).
- Note that Vlt < Vut and the difference between these two voltages is the hysteresis width Vh and can be written as

$$V_h = V_{ut} - V_{lt} = 2R2\ V_{sat}/(R1+R2)$$

Regenerative comparator (Schmitt trigger) cntd..

- The resistor R3 in figure 5.8(a) is chosen equal to R1||R2 to compensate for the input bias current.
- A non-inverting Schmitt trigger is obtained if Vi and Vref are interchanged in figure 5.8(a).

Voltage Regulators

- A voltage regulator is a circuit that supplies constant voltage regardless of changes in load currents
- Although voltage regulators can be designed using op-amps, it is quicker and easier to use IC voltage regulators.
- Furthermore, IC voltage regulators are versatile and relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short-circuit current limiting, thermal shutdown and floating operation for high voltage applications.

Voltage Regulators cntd..

- IC voltage regulator are of the following types
  - Fixed output voltage regulators: +ve and/or –ve output voltage
  - Adjustable output voltage regulators: +ve or –ve output voltage
  - Switching regulators
  - Special regulators
- Except for the switching regulators, all other types of regulators are called LINEAR regulators.
- The impedance of a linear regulator's active element may be continuously varied to supply a desired current to the load.
- On the other hand, in the switching regulator a switch is turned on and off at a rate such that the regulator delivers the desired average current in periodic pulses to the load.

Voltage Regulators cntd..

- Because the switching element dissipates negligible power in either the ON or OFF state, the switching regulator is more efficient than the linear regulator.
- Nevertheless, in switching regulators the power dissipation is substantial during the switching intervals (ON to OFF or OFF to ON). In addition, most loads can not accept the average current in periodic pulses. Therefore, most practical regulators are of the linear type.

Voltage Regulators cntd..

- Voltage regulators are commonly used for laboratory-type power supplies.
- Almost all power supplies use some type of voltage regulator IC because voltage regulators are simple to use, reliable, low in cost, and, above all, available in a variety of voltage and current ratings.

Performance Parameters

There are four typical performance parameters for voltage regulators. They are LINE regulation, LOAD regulation, temperature stability and ripple rejection.

- **LINE or INPUT regulation:** it is defined as the change in output voltage for a change in the input voltage and is usually expressed in milli volts or as a percentage of output voltage Vo.

Performance Parameters cntd..

- **LOAD Regulation:** It is the change in output voltage for a change in load current and is also expressed in milli volts or as a percentage of Vo
- **Temperature stability:** It is the change in output voltage per unit change in the temperature and is expressed in either milli volts/°C or parts per million (ppm)/°C

Performance Parameters cntd..

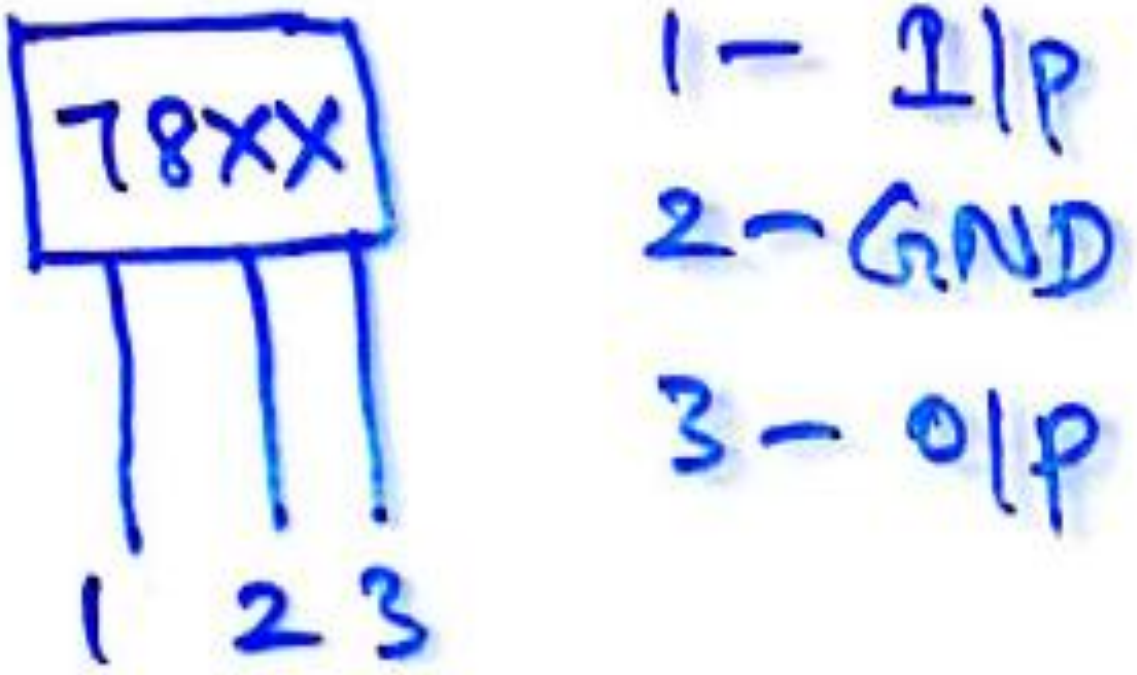
- **Ripple Rejection:** it is the measure of a regulator's ability to reject ripple voltages. It is usually expressed in decibels.
- The smaller the values of line regulation, load regulation and the temperature stability, the better the regulator.
- **Dropout Voltage:** It is the difference between input and output voltages.

Types of Voltage Regulators

- **Fixed Output Voltage Regulators:**
  - **Positive Output voltage regulator series:**

Device Type	O/P Voltage (Volts)	Max .Input Voltage (Volts)
7805	5.0	35
7806	6.0	35
7808	8.0	35
7812	12.0	35
7815	15.0	35
7818	18.0	35
7824	24.0	40

Types of Voltage Regulators cntd..

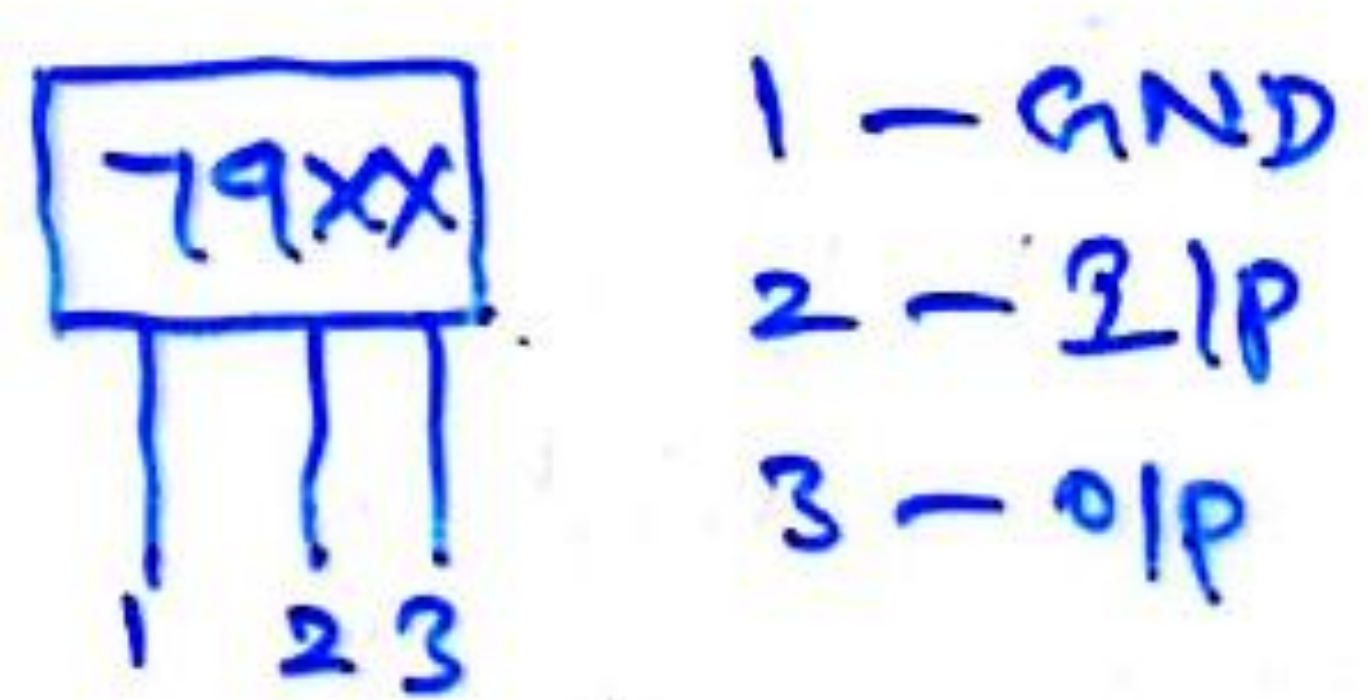


Types of Voltage Regulators cntd..

- **Negative Output voltage regulator series:**

Device Type	O/P Voltage (Volts)	Max .Input Voltage (Volts)
7902	-2.0	-35
7905	-5.0	-35
7905.2	-5.2	-35
7906	-6.0	-35
7908	-8.0	-35
7912	-12.0	-35
7915	-15.0	-35
7918	-18.0	-35
7924	-24.0	-40

Types of Voltage Regulators cntd..



Types of Voltage Regulators cntd..

Adjustable Output Voltage Regulators:

- In the case of fixed voltage regulators, for each voltage a separate device is to be used. This increases the inventory and hence the cost.
- Therefore, Adjustable voltage regulators came into picture. These regulators provide many voltages ranging from 1.2 to 57 volts.
- In addition, these have more versatility, more performance and more reliability than fixed voltage regulators.
- Adjustable +ve Voltage Regulators – LM317 and Adjustable –ve Voltage Regulators – LM337

Types of Voltage Regulators cntd..

Switching Regulators:

- Switching regulators are called so because these use a switch in the circuit.
- Switching regulators come in various circuit configurations including the Fly-back, Feed-forward, Push-pull, and non-isolated single-ended or single-polarity types.
- Switching regulators can operate in any of three modes: Step-up, step-down or polarity inverting.
- Switching regulator is often referred to as a DC transformer.
- Eg: IC μA78S40 from Fairchild.

Types of Voltage Regulators cntd..

Special Regulators:

- It is used as
  - Voltage References: It is used as a reference voltage in A/D and D/A converters
  - Voltage Inverter: It is used in Data Acquisition and Microprocessor-based systems in which a +ve supply is available and an additional –ve supply is required.

IC 723 Regulator and It's Features

- 3 terminal voltage regulators are capable of producing only fixed +ve or –ve output voltages. Moreover, such regulators do not have short circuit protection.
- Therefore these 3 terminal regulators evolved into dual polarity variable voltage regulators and further evolved into the monolithic linear voltage regulators and monolithic switching regulators.
- One example for monolithic linear voltage regulator is IC723.
- IC723 general purpose regulator overcomes the limitations of 3 terminal fixed voltage regulators
- IC723 is a low current device.

Types of Voltage Regulators cntd..

- 150 mA o/p current without external pass transistor.
- o/p currents in excess of 10A possible by adding external transistors
- Input voltage 40 V maximum.
- O/p voltage adjustable from 2V to 37 V.
- Can be used as either a linear or a switching regulator.

Limitations: it has no built-in thermal protection.

End of Unit I

Unit II

Op-Amp, IC-555 & IC 565 Applications

Introduction to Filters

- Based on the components used in the circuit the filters are divided into following categories.
  - Active filters
  - Passive filters

Active Filters:

- Active filters employ transistors or op-amps in addition to resistors and capacitors.

Passive Filters:

- Here the type of element used dictates the operating frequency range of the filter.

Introduction to Filters cntd..

Eg:

- RC filters are used for audio or low frequency operation.
- LC or Crystal filters are used at RF or High frequencies.

An active filter offers the following advantages over a Passive filter.

- **Gain and Frequency adjustment flexibility:** Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. In addition, the active filter is easier to tune or adjust.

Introduction to Filters cntd..

- **No Loading problem:** Because of the high input resistance and low output resistance of the op-amp, the active filter does not cause loading of the source or load.
- **Cost:** Typically, active filters are more economical than passive filters. This is because of the variety of cheaper op-amps and the absence of the inductors.

Introduction to Filters cntd..

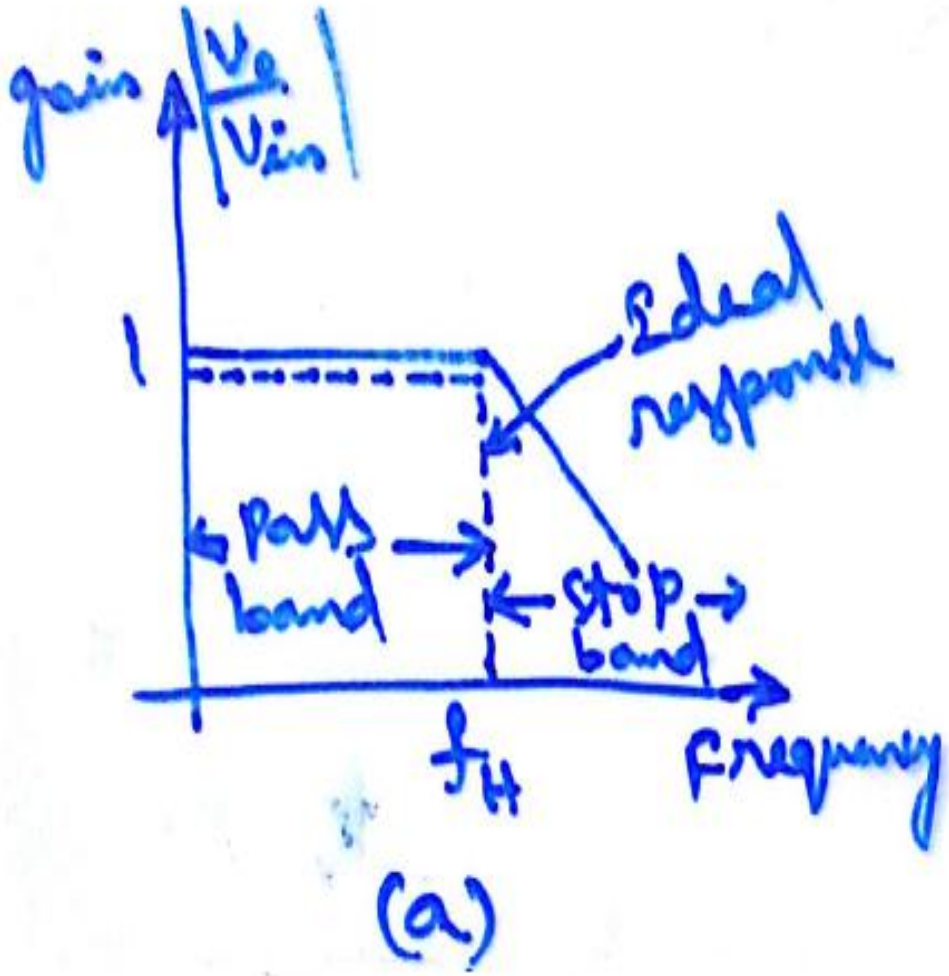
- Although active filters are most extensively used in the field of Communications and Signal processing, they are employed in one form or another in almost all sophisticated electronic systems.
- The different systems that use Active filters are Radio, television, telephone, Radar, Space satellites, and bio-medical equipment.
- Based on the operating frequency the filters are classified as follows.

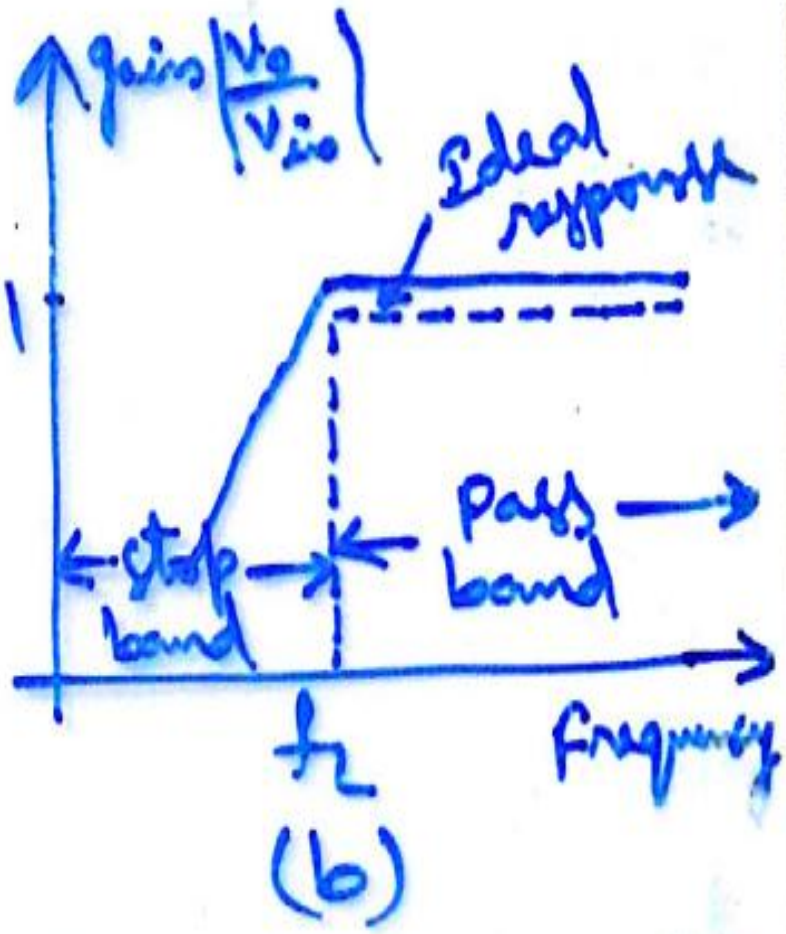
Introduction to Filters cntd..

- Low pass filter
- High pass filter
- Band pass filter
- Band stop filter
- All pass filter

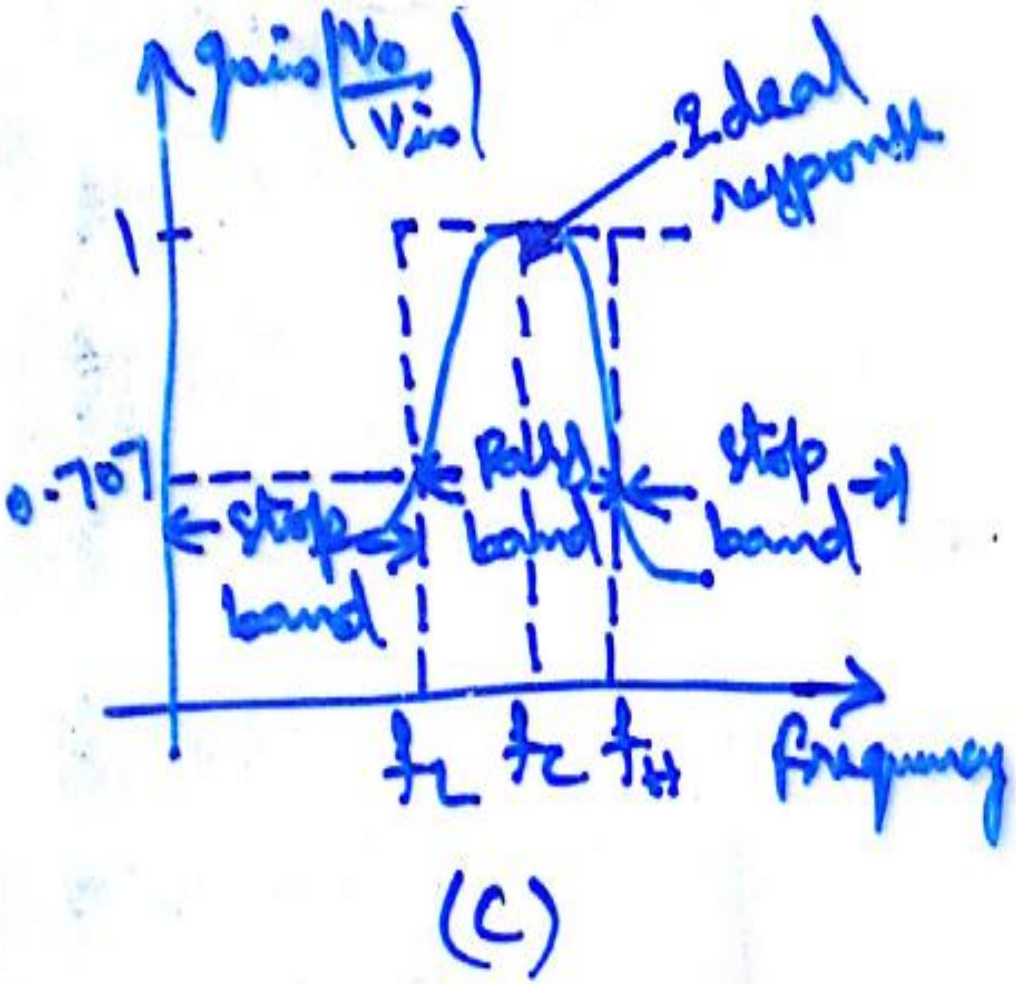
- Each of these filters uses an op-amp as an active element and resistors and capacitors as passive elements.
- Figure 8.1 shows the frequency response characteristics of the five types of filters.

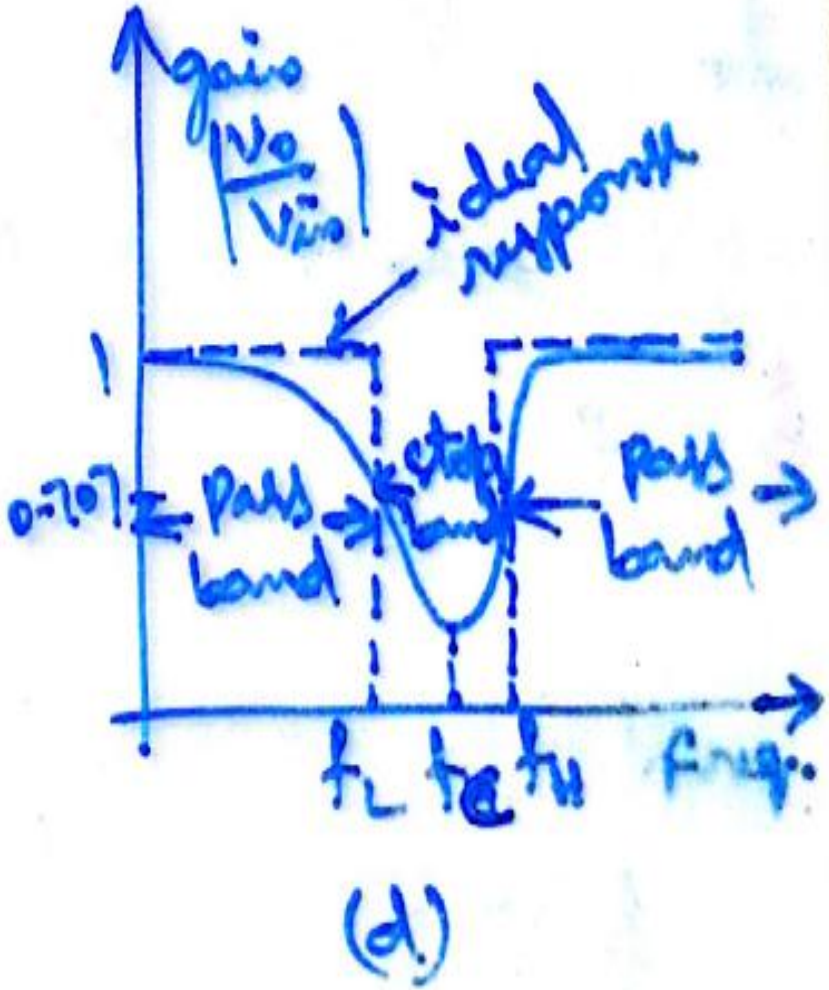
Introduction to Filters cntd..



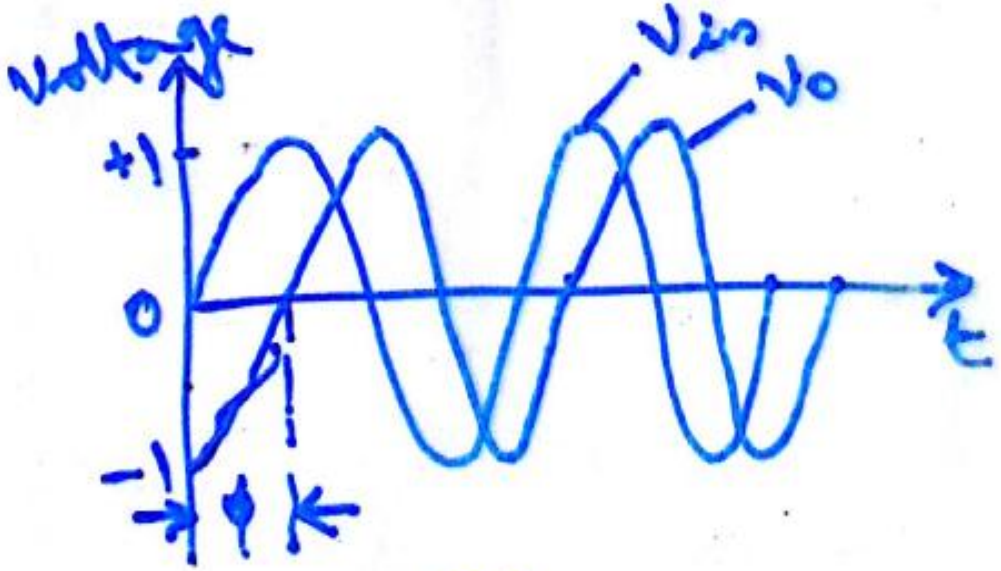


Introduction to Filters cntd..





Introduction to Filters cntd..



(e)

Fig 4.1 Frequency response of major active filters
(a) Low-pass (b) High pass (c) Band pass
(d) Band-reject (e) phase shift b/w i/p & o/p voltages of an all pass filter

Introduction to Filters cntd..

- Figure 8-1(a) shows the frequency response of low pass filter. As indicated by dashed line, an ideal filter has a zero loss in its pass band and infinite loss in its stop band
- Unfortunately, ideal filter response is not practical. However, it is possible to obtain a practical response that approximates the ideal filter response by using special design techniques as well as precision component values and high speed op-amps.
- Butterworth, chebyshev and caver filters are some of the most commonly used practical filters that approximate the ideal response.

Introduction to Filters cntd..

- The key characteristics of Butterworth filters is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat-flat filter.
- Figure 8-1(b) shows a high pass filter with a stop band $0 < f < fL$ and pass band $f > fL$.
- A band pass filter has a pass band between two cut-off frequencies fH and fL, where $fH > fL$ and two stop bands $0<f<fL$ and $f>fH$.

Band width of the band pass filter – fH-fL.

Introduction to Filters cntd..

- The band reject filter performs exactly opposite to the band pass, ie it has a band stop between two cut off frequencies fH and fL and two pass bands 0<f<fL and f>fH.
- The band reject filter is also called as band stop or band elimination filter
- Figure 8-1(e) shows the phase shift between input and output voltages of an all pass filter. This filter passes all frequencies equally well ie input and output voltages are equal in amplitude for all frequencies, with the phase shift between the two a function of frequency.

Introduction to Filters cntd..

- As shown figure 8-1 (a) – (d), the actual response curves of the filters in the stop band either steadily decrease or increase or both with increase in frequency.
- The rate at which the gain of the filter changes in the stop band is determined by the order of the filter.
- For first order low pass filter, gain decreases by 20 dB/decade in the stop band.
- For second order low pass filter, gain decreases by 40 dB/decade in the stop band.

Introduction to Filters cntd..

- By contrast, for first order high pass filter, gain increases by 20 dB/decade in the stop band.
- For second order high pass filter, gain increases by 40 dB/decade.

First Order Low pass Butterworth filter

- Figure 8-2 shows a first order low pass Butter worth filter that uses an RC network for filtering. Note that the op-amp is used in the non-inverting configuration, hence it does not load down the RC network. Resistors R1 and Rf determine the gain of the filter.

First Order Low Pass Butterworth filter cntd..

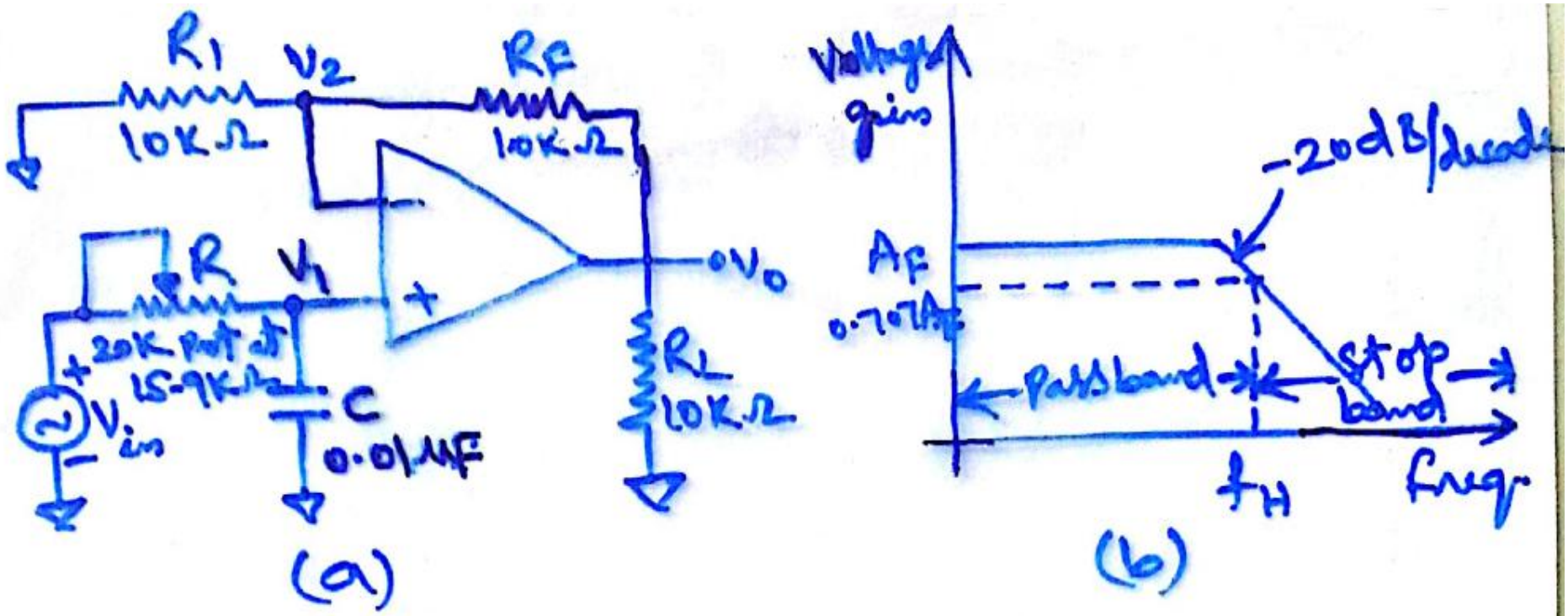


Fig 8.2 First-order low-pass Butterworth filter (a) circuit (b) frequency response.

First Order Low Pass Butterworth filter cntd..

- According to the voltage divider rule, the voltage at the non-inverting terminal (across capacitor C) is

$$V1 = -jXc/(R-jXc)\ Vin \quad \text{-------- eq(1)}$$

where $j=\sqrt{-1}$ and $-jXc = 1/j2\pi fC$

simplifying eq(1), we get

$V1 = Vin / 1+ j2\pi fRC$

Output voltage $Vo= (1 + (Rf/R1))\ V1$

ie $Vo = (1+(Rf/R1))\ (Vin/(1+j2\pi fRC))$

First Order Low Pass Butterworth filter cntd..

$$V_o/V_{in} = A_f/(1+j\,(f/f_H)) \quad \text{------ eq(2)}$$

where V_o/V_{in} = gain of the filter as a function of frequency.

$A_f = 1 + (R_f/R_1)$ = pass band gain of the filter

f = frequency of the input signal

$f_H = 1/2\pi RC$ = high cutoff frequency of the filter.

First Order Low Pass Butterworth filter cntd..

- The gain magnitude and phase angle equations of the low pass filter can be obtained by converting eq(2) into it's equivalent polar form, as follows.

$$|Vo/Vin| = Af/\sqrt{(1+(f/fH)^2)} \text{ ----- eq(3)}$$

$$\phi = - \tan^{-1}(f/fH)$$

Where ϕ is the phase angle in degrees

- The operation of the low pass filter can be verified from the gain magnitude equation (3).

First Order Low Pass Butterworth filter cntd..

- At very low frequencies, that is, f<fH
  $|Vo/Vin| = Af$
- At f = fH, $|Vo/Vin| = 0.707\ Af$
- At f>fH, $|Vo/Vin| < Af$
- Thus the low pass filter has a constant gain Af from 0 Hz to the almost high cutoff frequency fH
- At fH, the gain is 0.707 Af, and after fH it decreases at a constant rate with as increase in frequency [see fig 8-2 b]

First Order Low Pass Butterworth filter cntd..

- The frequency f =fH is called the cutoff frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz.
- Other equivalent terms for cut off frequency are -3dB frequency, break frequency or corner frequency.

Filter Design

A low pass filter can be designed by implementing the following steps

First Order Low Pass Butterworth filter cntd..

1 Choose a value of high cut off frequency fH

2 Select a value of C less than or equal to 1 μF

(Mylar or tantalum capacitors are recommended for better performance)

3 Calculate the value of R using $R = 1/2\pi fH\ C$

4 Finally, select values of R1 anf Rf dependant on the desired pass band gain Af using

$Af = 1 + (Rf/R1)$

First Order Low Pass Butterworth filter cntd..

Example 1: Design a low pass filter at a cut off frequency of 1 KHz with a pass band gain of 2

Solution:

Follow the preceding design steps

1 fH = 1 KHz

2 Let C = 0.01 μF

3 Then R = 1/2 Π (10^3) (10^-8) = 15.9 KΩ (use a 20 KΩ pot.)

4 Since the pass band gain is 2, R1 and Rf must be equal. Therefore, let R1 = Rf = 10 KΩ

The complete circuit with components values is shown in Fig 8-2 a.

First Order Low Pass Butterworth filter cntd..

Frequency Scaling

- Once a filter is designed there may sometimes be a need to change its cut off frequency. The procedure used to convert an original cut off frequency fH to a new cut off frequency fH1 is called frequency scaling.
- Frequency scaling is accomplished as follows
- To change a high cut off frequency, multiply R or C but not both, by the ratio of original cut off frequency to new cut off frequency.

First Order Low Pass Butterworth filter cntd..

Example 2:

Using the frequency scaling technique, convert 1 KHz cut off frequency of the low pass filter of Example 1 to a cut off frequency of 1.6 KHz

Solution: To change a cut off frequency from 1 KHz to 1.6 KHz, we multiply the 15.9 KΩ resistor by

Original cut off frequency/new cut off frequency = 1 KHz/1.6 KHz = 0.625

Therefore, new resistor R = 15.9 KΩ * 0.625 = 9.94 KΩ

However, 9.94 KΩ is not a standard value.

First Order Low Pass Butterworth filter cntd..

Therefore, use R= 10KΩ potentiometer and adjust it to 9.94 KΩ.

Thus the new cut off frequency is

$$f_{H1} = 1/ 2\pi (0.01\ \mu F) (9.94\ K\Omega) = 1.6\ KHz.$$

First Order High Pass Butterworth filter

- High pass filters are often formed simply by interchanging the frequency-determining resistors and capacitors in low pass filters.
- That is, a first order high pass filter is formed from a first order low pass type by interchanging components R & C.
- Figure 8.6 shows a first order high pass Butter worth filter with a low cut off frequency of fL. This is the frequency at which the magnitude of the gain is 0.707 times its pass band value.

First Order High Pass Butterworth filter cntd..

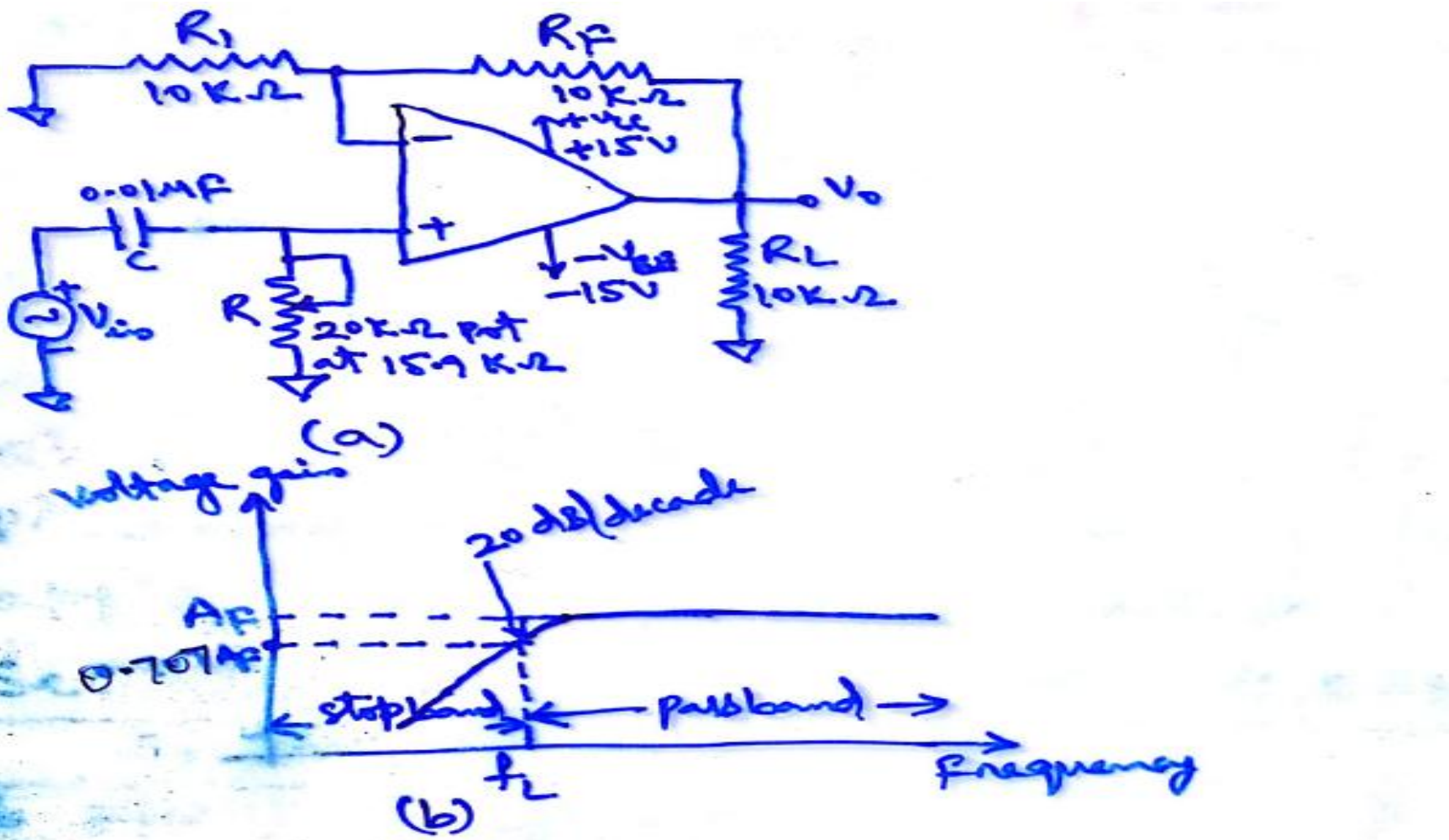


fig 8-6 (a) First-order high-pass Butterworth filter (b) It's frequency response.

First Order High Pass Butterworth filter cntd..

- Obviously all frequencies higher than fL are pass band frequencies, with the highest frequency determined by the closed loop band width of the op-amp.
- For the first order high pass filter of Figure 8.6a, the output voltage is

$$V_o = (1+(R_f/R_1))\ (j2\pi fRC/(1+j2\pi fRC))\ V_{in}$$

$$V_o/V_{in} = A_f[j(f/f_L)/(1+j(f/f_L))$$

where $A_f = 1+(R_f/R_1)$, & $f_L = 1/2\pi RC$

Hence the magnitude of the voltage gain is

$$|V_o/V_{in}| = A_f\ (f/f_L)/\sqrt{(1+(f/f_L)^2)}$$

First Order High Pass Butterworth filter cntd..

- Since the high pass filters are formed from low pass filters simply by interchanging Rs and Cs, the design and frequency scaling procedures of the low pass filters are also applicable to high pass filters.

Wave form Generators

There are different types of wave form generators which are given below.

1 Square wave generator

2 Triangular wave generator

3 Saw tooth wave generator

Square wave Generator (Astable Multivibrator)

- A simple op-amp square wave generator is shown in Figure 5.10a.

Square wave generator

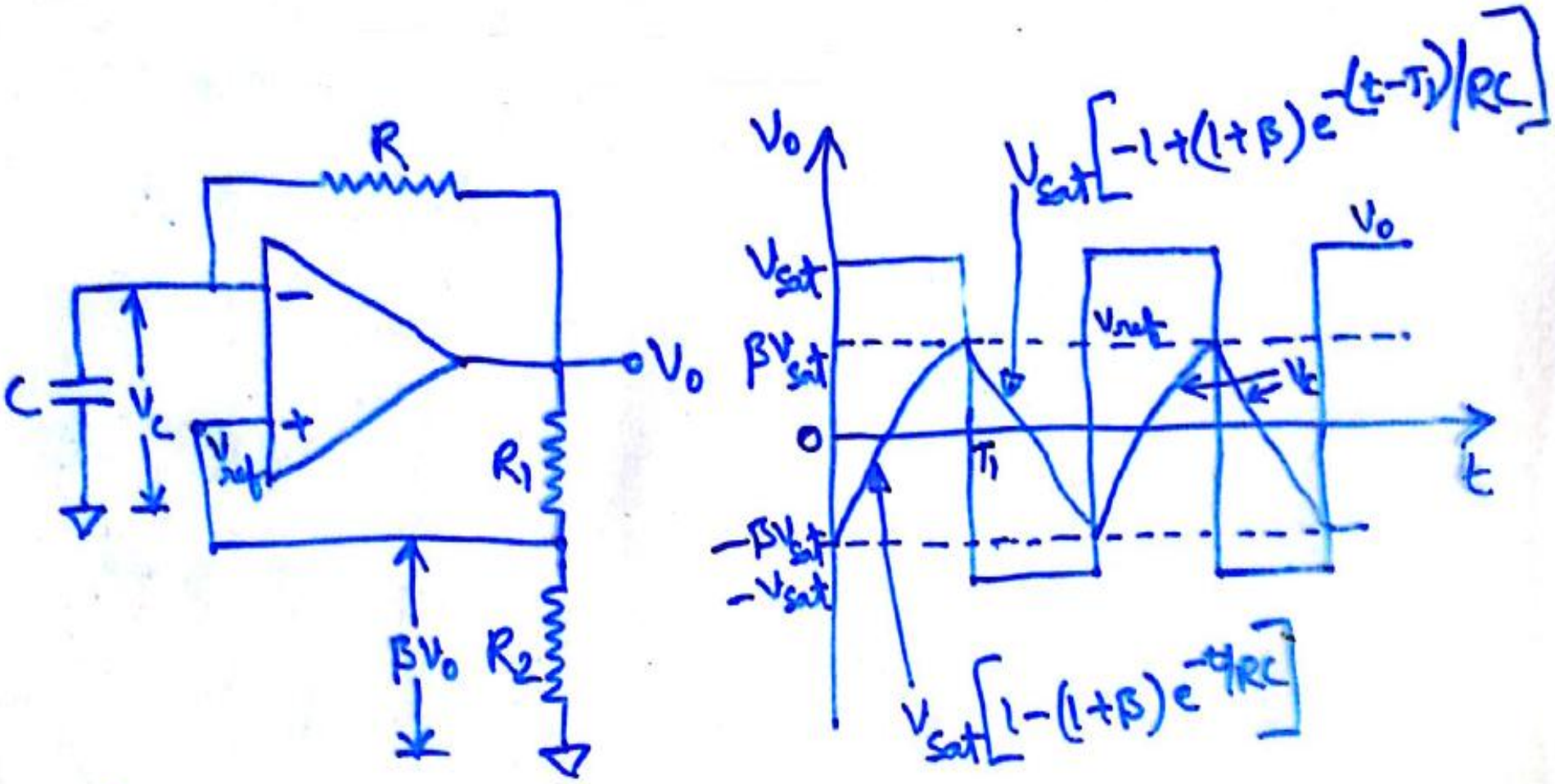


Fig 5.10(a) Simple op-amp square wave generator (b) waveforms.

Square wave generator cntd..

- It is also called a Free running oscillator.
- The principle of generation of square wave output is to force an op-amp to operate in saturation region.
- In Figure 5.10(a), fraction $\beta = R2/(R1+R2)$ of the output is fed back to the +ve input terminal. Thus the reference voltage Vref is βVo and may take values as $+\beta Vsat$ or $-\beta Vsat$.

Square wave generator cntd..

- The output is also fed back to the –ve input terminal after integrating by means of a low pass RC combination.
- Whenever input at the –ve input terminal just exceeds Vref, switching takes place resulting in a square wave output.
- In Astable multivibrator, both the states are quasi stable.

Square wave generator cntd..

Frequency Derivation

The frequency is determined by the time it takes the capacitor to charge from –βVsat to + βVsat and vice versa.

The voltage across the capacitor as a function of time is given by

$$Vc(t) = Vf + (Vi – Vf)\, e^{-t/RC}$$

where, the final value, Vf = +Vsat

and the initial value, Vi = –βVsat

Therefore $Vc(t) = +Vsat + (–\beta Vsat – Vsat)\, e^{-t/RC}$

$$Vc(t) = Vsat – Vsat(1+\beta)\, e^{-t/RC}$$

At t = T1, voltage across the capacitor reaches βVsat and switching takes place.

Square wave generator cntd..

- Therefore

  $V_c(T1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)\, e^{-T1/RC}$

After algebraic manipulation, we get

$T1 = RC \ln (1+\beta)/(1-\beta)$

This gives only one half of the period.

Therefore the total time period, $T = 2*T1 = 2RC \ln (1+\beta)/(1-\beta)$ and the output waveform is symmetrical.

If R1 = R2, then $\beta = 0.5$ and $T = 2RC \ln 3$ and

for R1=1.16 R2, it can be seen that

$T = 2RC$ or $f_o = 1/2RC$

Triangular Wave Generator

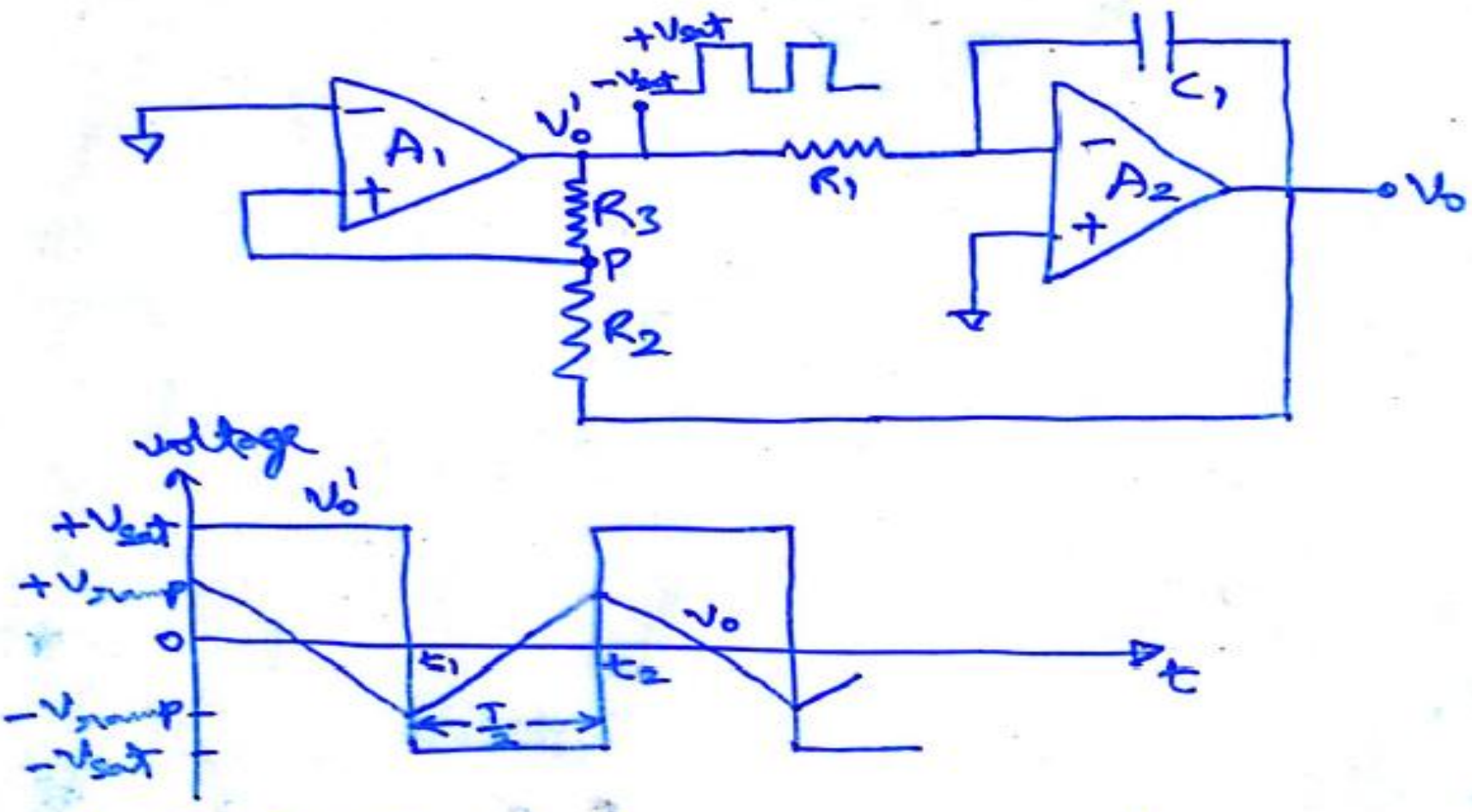


Fig 5-13 (a) Triangular waveform generator (b) waveforms.

Triangular Wave Generator cntd..

- It basically consists of a two level comparator followed by an integrator.
- The output of the comparator A1 is a square wave of amplitude + or – Vsat and is applied to the –ve input terminal of the integrator A2 producing a triangular wave. This triangular wave is fed back as input to the comparator A1 through a voltage divider R2R3.

Triangular Wave Generator cntd..

- Initially, let us consider that the output of the comparator A1 is at +Vsat. The output of the integrator A2 will be a –ve going ramp as shown in figure 5.13b. This one end of the voltage divider R2R3 is at a voltage +Vsat and the other at the –ve going ramp of A2.
- At a time t=t1, when the –ve going ramp attains a value of –Vramp, the effective voltage at point p becomes slightly less than 0 volts. This switches the output of A1, from positive saturation level to negative saturation level – Vsat.

Triangular Wave Generator cntd..

- During the time when the output of A1 is at -Vsat, the output of A2 increases in the positive direction.
- And at the instant t=t2, the voltage at point p becomes just above 0 volts, thereby switching the output of A1 from –Vsat to +Vsat. The cycle repeats and generates a triangular waveform.
- It can be seen that the frequency of the square wave and triangular wave will be the same.
- However, the amplitude of the triangular wave depends upon the RC value of the integrator A2 and output voltage level of A1.

Triangular Wave Generator cntd..

Derivation of Frequency of Triangular Waveform

- The effective voltage at point p during the time when output of A1 is at +Vsat level is given by

$-V_{ramp}+(R2/(R2+R3))\ [+V_{sat} – (-V_{ramp})]$ -- Eq(1)

At t=t1, the voltage at point p becomes approximately equal to zero. Therefore from Eq(1), we get $-V_{ramp} = (-R2/R3)\ (+V_{sat})$

Similarly at t=t2, when the output of A1 switches from –Vsat to +Vsat

$V_{ramp} = (-R2/R3)\ (-V_{sat}) = (R2/R3)\ V_{sat}$

Triangular Wave Generator cntd..

Therefore peak to peak amplitude of the triangular wave is

$V_o(pp) = +V_{ramp} - (-V_{ramp})$

$V_o(pp) = 2 V_{ramp} = 2 (R2/R3) V_{sat}$ ---- Eq(2)

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period T/2.

Putting the values in the basic integrator equation $V_o = -(1/RC) \int V_i \, dt$, we get

$V_o(pp) = -(1/R1C1) \int_0^{T/2} (-V_{sat}) dt = (V_{sat}/R1C1) (T/2)$

Therefore $T = 2 R1C1 V_o(pp)/V_{sat}$

Putting the value of $V_o(pp)$ from Eq(2), we get

$$T = 4R1 C1 R2/R3$$

Triangular Wave Generator cntd..

Hence the frequency of oscillation fo is

$$fo = 1/T = R3/4\ R1\ C1\ R2$$

Sawtooth Wave Generator

- The difference between the triangular and sawtooth waveforms is that

rise time and fall time are equal – Triangular

rise time and fall time are unequal – Sawtooth

- The triangular wave generator can be converted into a sawtooth wave generator by injecting a variable DC voltage into the non-inverting terminal of the integrator A2.
- This can be accomplished by using the potentiometer and connecting it to the +Vcc and -Vee as shown in Figure 8-24(a)

Sawtooth Wave Generator cntd..

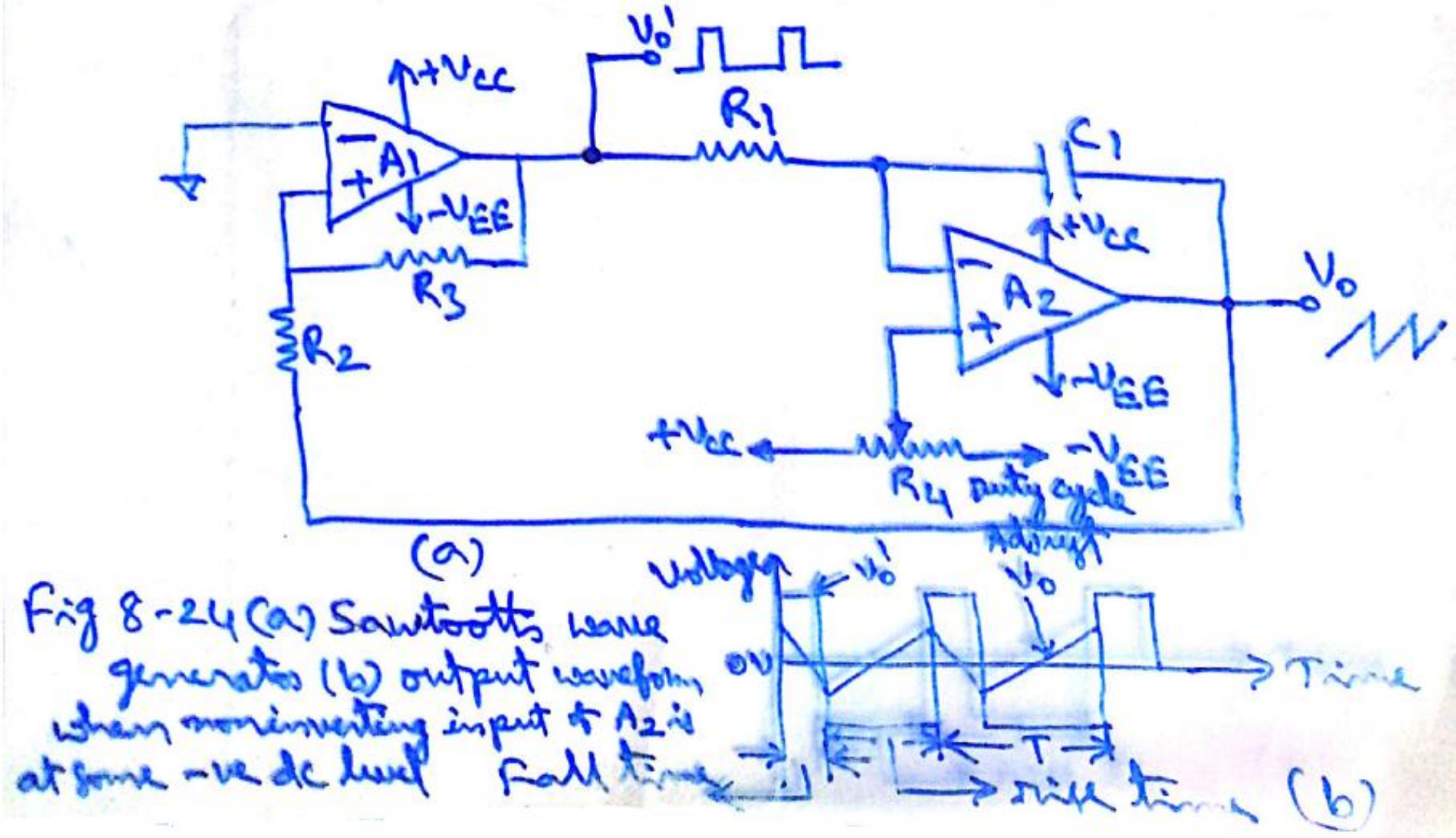


Fig 8-24 (a) Sawtooth wave generator (b) output waveform when noninverting input of A_2 is at some -ve dc level

Sawtooth Wave Generator cntd..

- Depending on the R4 setting, a certain DC level is inserted in the output of A2.
- Now suppose that the output of A1 is a square wave and the potentiometer R4 is adjusted for a certain DC level.
- This means that the output of A2 will be a triangular wave, riding on some DC level that is a function of the R4 setting.
- The duty cycle of the square wave will be determined by the polarity and amplitude of this DC level.
- A duty cycle less than 50% will then cause the output of A2 to be a sawtooth.

Sawtooth Wave Generator cntd..

- With the wiper at the center of R4, the output of A2 is a triangular wave. For any other position of R4 wiper, the output is a sawtooth waveform.

R4 wiper is towards **–Vee**,the **rise time is more**

R4 wiper is towards **+Vcc**,the **fall time is more**

Introduction to IC 555 Timer

- The 555 timer is a highly stable device for generating accurate time delay or oscillation.
- Signetics corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8 pin circular type, To-99 can or 8-pin mini DIP or as 14–pin DIP.
- A single 555 timer can provide time delay ranging from µsec to hours.
- The 555 timer can be used with supply voltage in the range of +5 Volts to +18 volts and can drive load upto 200mA.
- It is compatible with both TTL and CMOS logics.

Introduction to IC 555 Timer cntd..

- Because of wide range of supply voltage, the 555 timer is versatile & easy to use in various applications.
- Various applications include oscillators, pulse generator, ramp & square wave generator, mono shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

Functional Diagram of 555 Timer

- Figure 8.2 gives the functional diagram for 555 IC timer.

Functional Diagram of 555 Timer

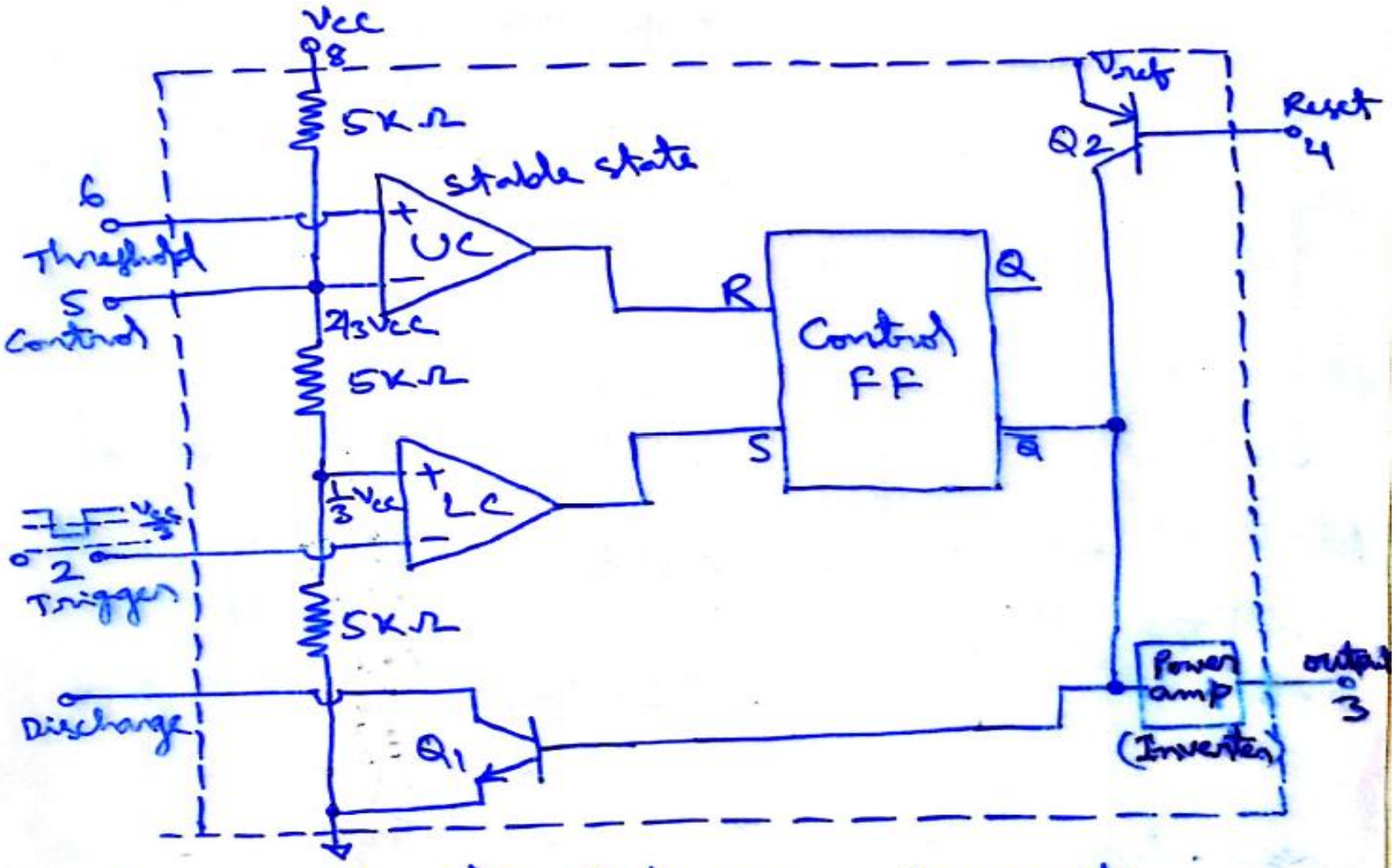


Fig 8.2 Functional diagram of 555 timer

Functional Diagram of 555 Timer cntd..

- Referring to Figure 8.2, 3 5KΩ internal resistors act as voltage divider, providing bias voltage of 2/3 Vcc to the upper comparator (UC), and 1/3 Vcc to the lower comparator (LC) where Vcc is the supply voltage.
- In the stand by(stable) state, the output $\overline{Q}$ of control filp-flop(FF) is high.
- This makes the output LOW because of power amplifier which behaves like inverter.
- A –ve going trigger pulse is applied to pin 2 and should have its DC level greater than the threshold level of the lower comparator (that is Vcc/3).

Functional Diagram of 555 Timer cntd..

- At the –ve going edge of the trigger, as the trigger passes through Vcc/3, the output of the lower comparator goes HIGH and sets the FF.
- During the positive excursion, when the threshold voltage at pin 6 passes through 2/3 Vcc, the output of the upper comparator goes HIGH and resets the FF($Q=0$, $\overline{Q}=1$).
- The reset input (pin 4) provide a mechanism to reset the FF in a manner which over rides the effect of any instruction coming to FF from lower comparator.
- When this reset is not used, it is returned to Vcc

Monostable Operation

- Figure 8.3 shows a 555 timer connected for mono stable operation and its functional diagram is shown in Figure 8.4

Monostable Operation cntd..

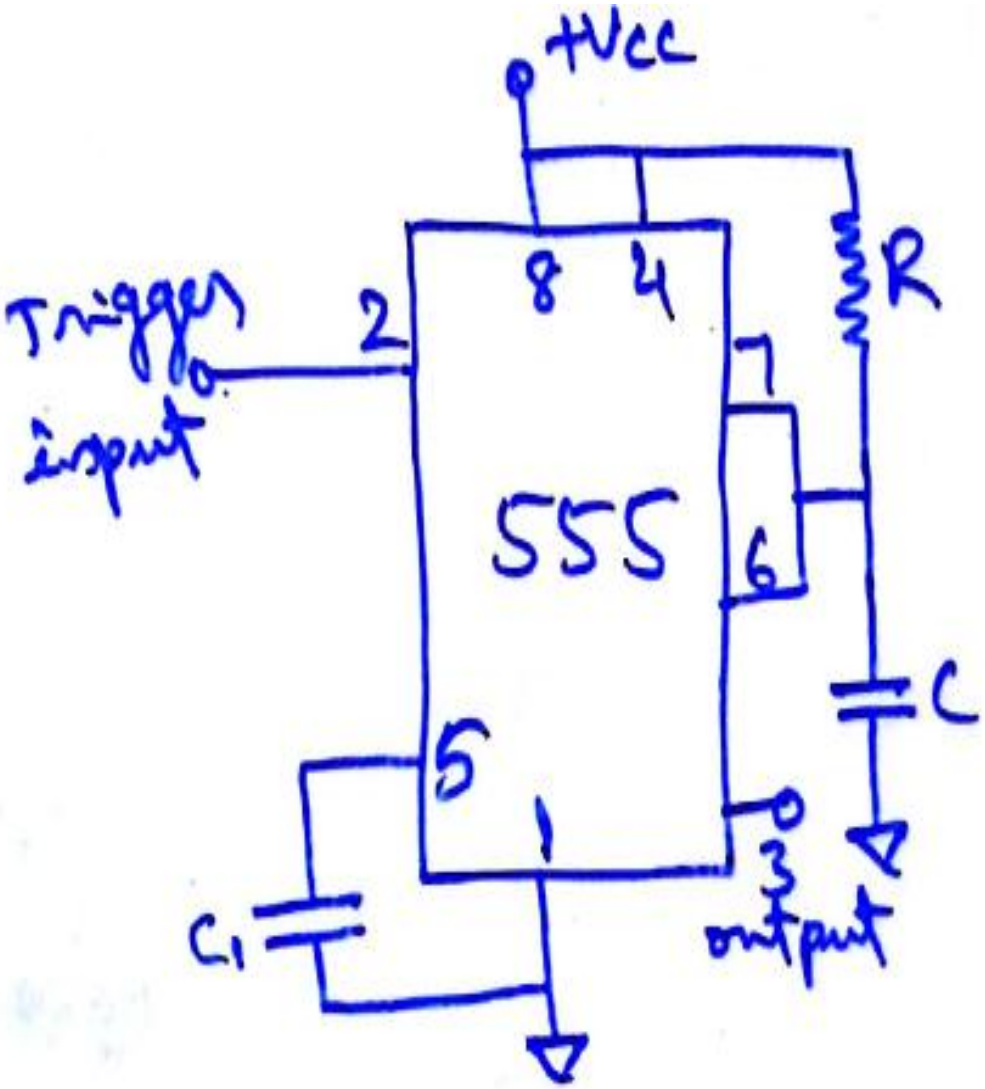


Fig 8-3 Monostable multivibrator

Monostable Operation cntd..

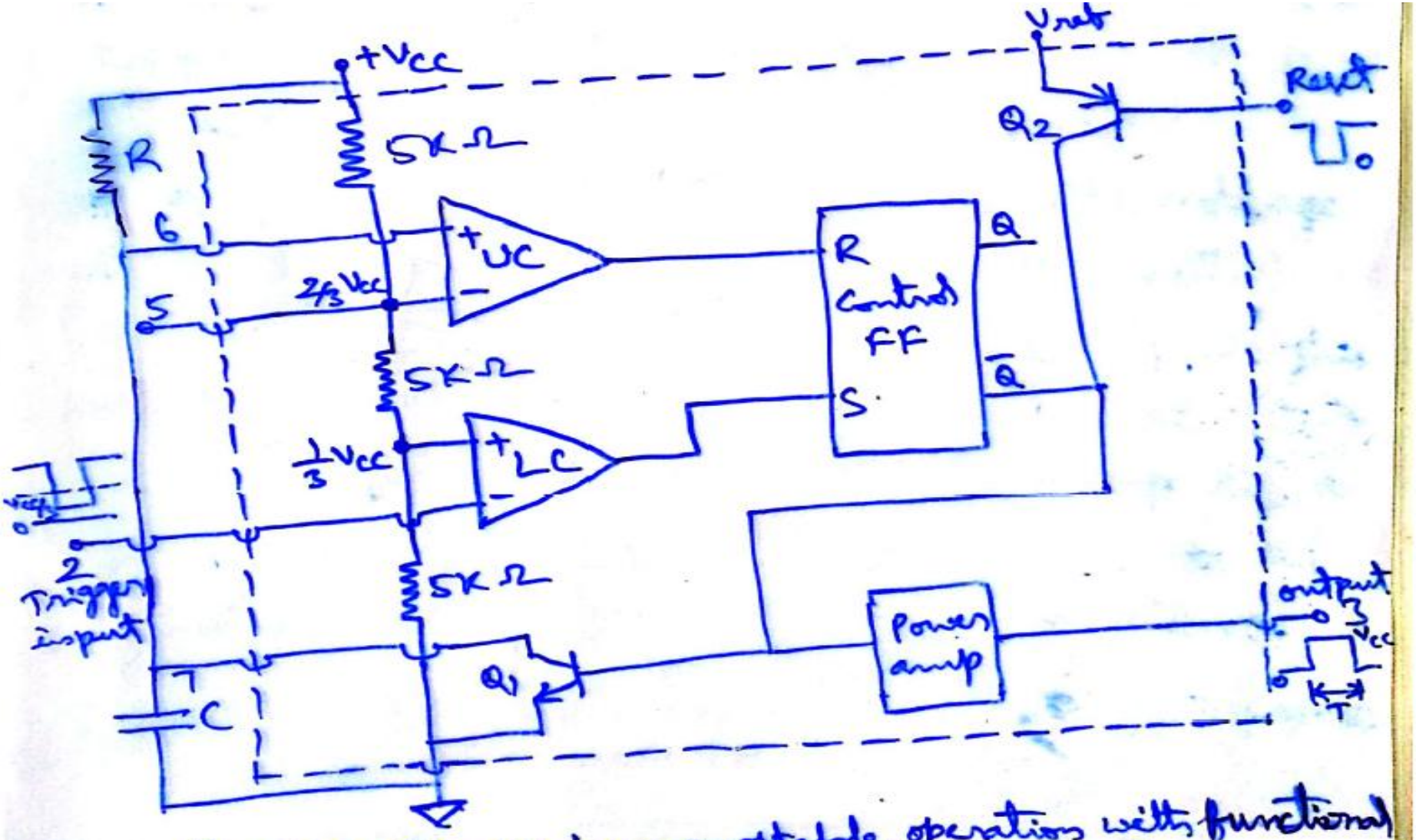


Fig 8-4 Timer in monostable operation with functional diagram.

Monostable Operation cntd..

- In the stand by state, FF holds transistor Q1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential ie low.
- As the trigger passes through Vcc/3, the FF is set ie $\overline{Q} = 0$. This makes the transistor Q1 off and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is low, output goes HIGH (= Vcc).
- Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC as in Figure 8.5 b.

Monostable Operation cntd..

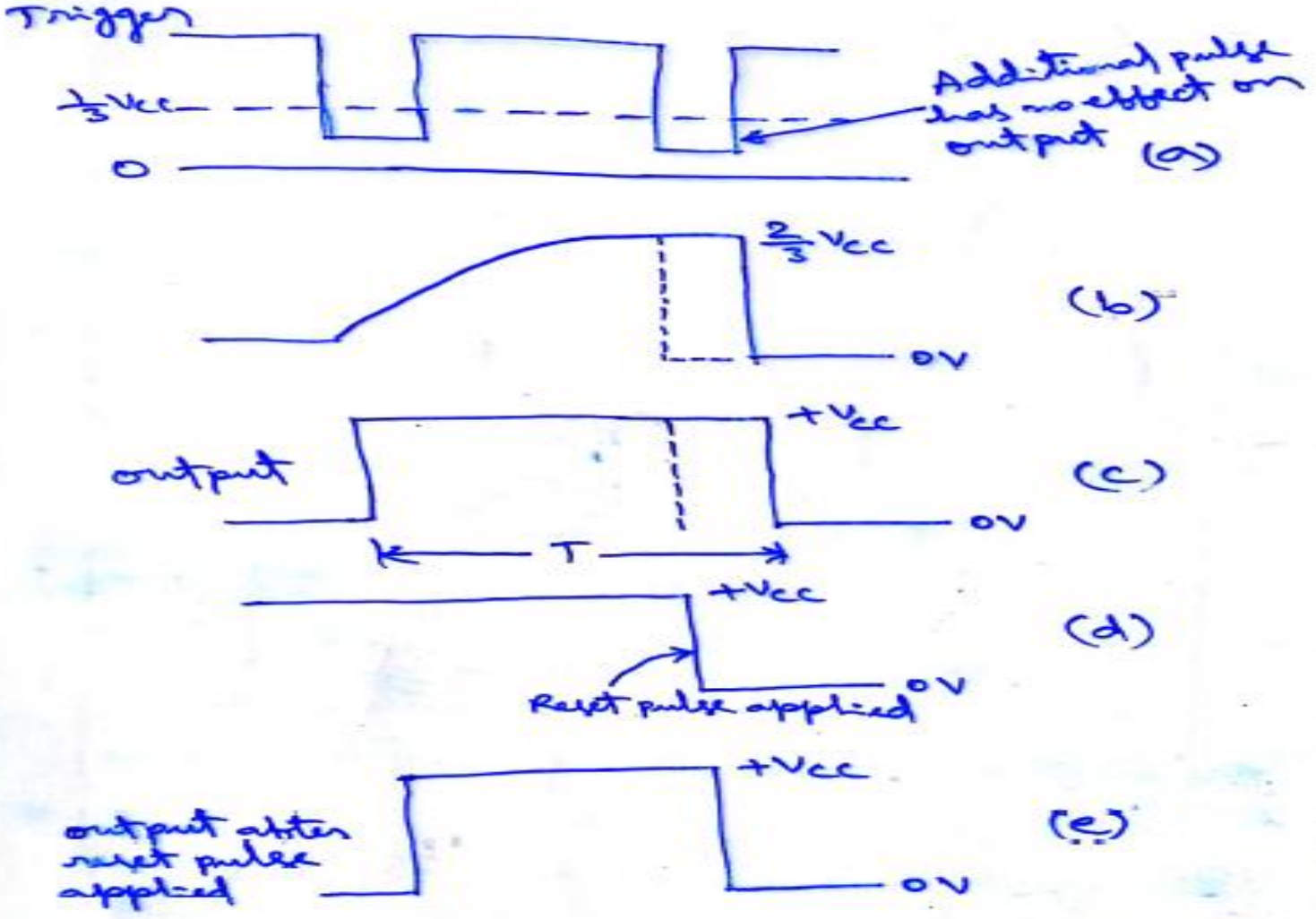


Fig 8.5. Timing pulses.

Monostable Operation cntd..

- After a time period T the capacitor voltage is just greater than 2/3 Vcc and the upper comparator resets the FF, that is, R =1, S=0. This makes Q = 1, transistor Q1 goes on (ie saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the ground potential as shown in Figure 8.5c.
- The voltage across the capacitor as in Figure 8.5b is given by $V_c = V_{cc}(1- e^{-t/RC})$

At t= T, $V_c = 2/3\ V_{cc}$

Therefore $2/3\ V_{cc} = V_{cc}(1- e^{-T/RC})$

Monostable Operation cntd..

e^-T/RC = 1 - 2/3 ==> e^T/RC = 3

T/RC = ln3 ➔ T = 1.1 RC ------- Eq(1)

- It is evident from Eq(1) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state.
- However, if a negative going reset pulse as in Figure 8.5 d is applied to the reset terminal during the timing cycle, transistor Q2 goes off, Q1 becomes on and the external timing capacitor C is immediately discharged. The output now will be as in Figure 8.5 e.

Applications in Monostable Mode

- Some applications of monostable multivibrator are
  - Missing pulse detector
  - Linear ramp generator

Missing Pulse Detector:

- Missing pulse detector circuit using 555 timer is shown in Figure 8.8.

Applications in Monostable Mode cntd..

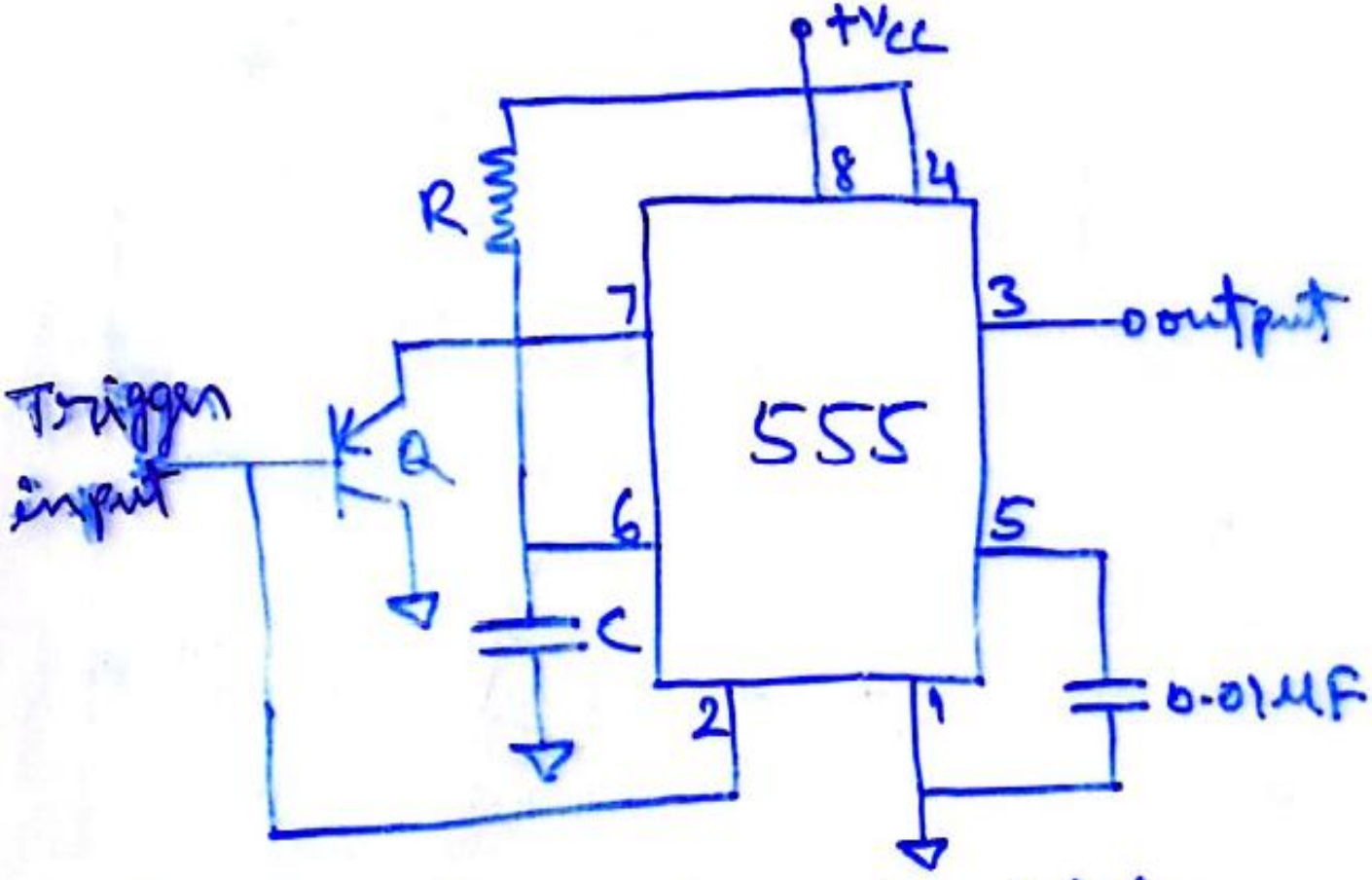


Fig 8-8. A missing pulse detector monostable ckt.

Applications in Monostable Mode cntd..

- Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~0.7V). The output of the timer goes HIGH.
- So long the trigger pulse train keeps coming at pin 2, the output remains HIGH.
- However, if a pulse misses, the trigger input is high and transistor Q is cutoff. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot.
- Thus this type of circuit can be used to detect missing heart beat.

Applications in Monostable Mode cntd..

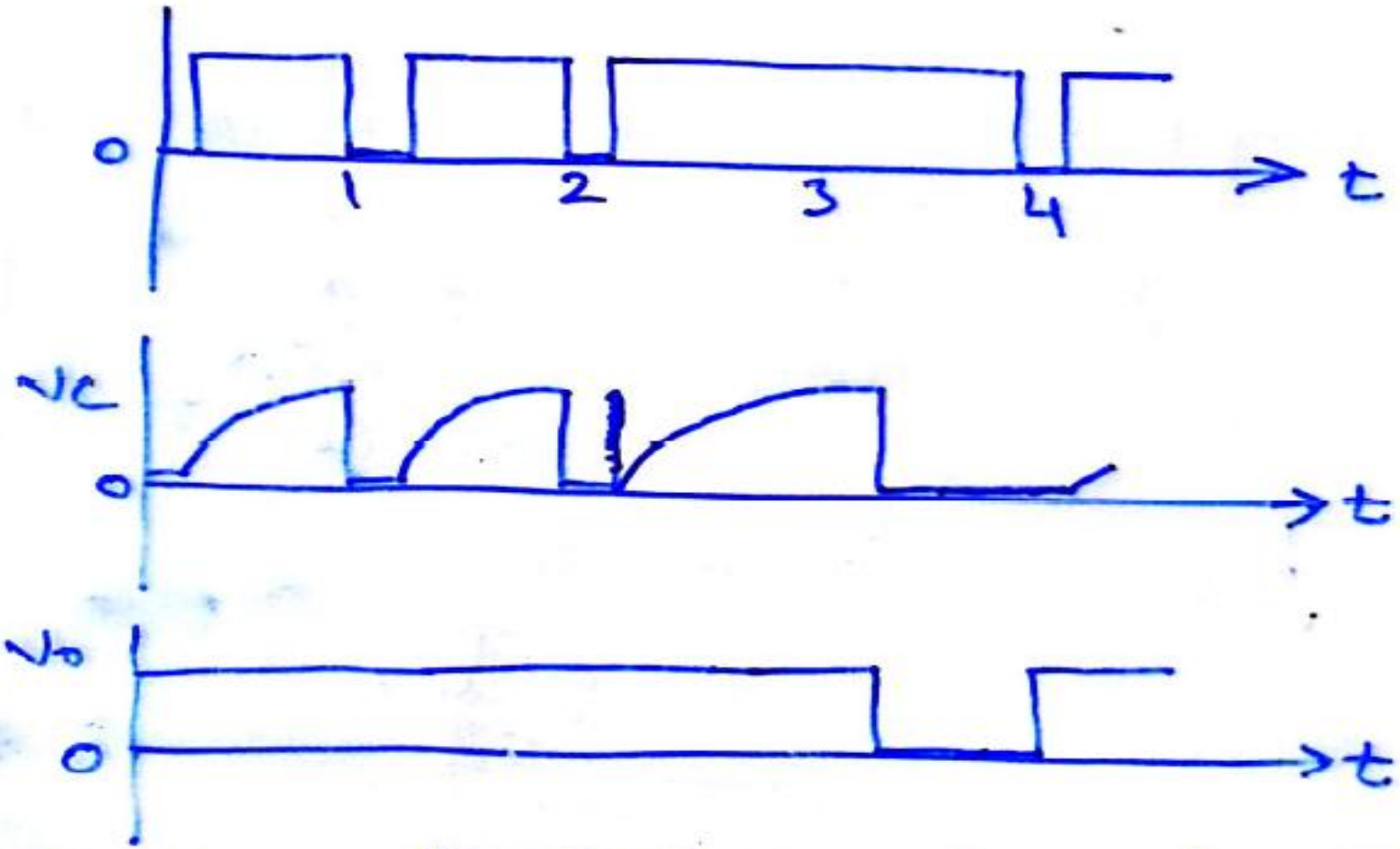


Fig 8-9 output of missing pulse detector

Astable Operation

- The device is connected for Astable operation as shown in Figure 8.15.

Astable Operation cntd..

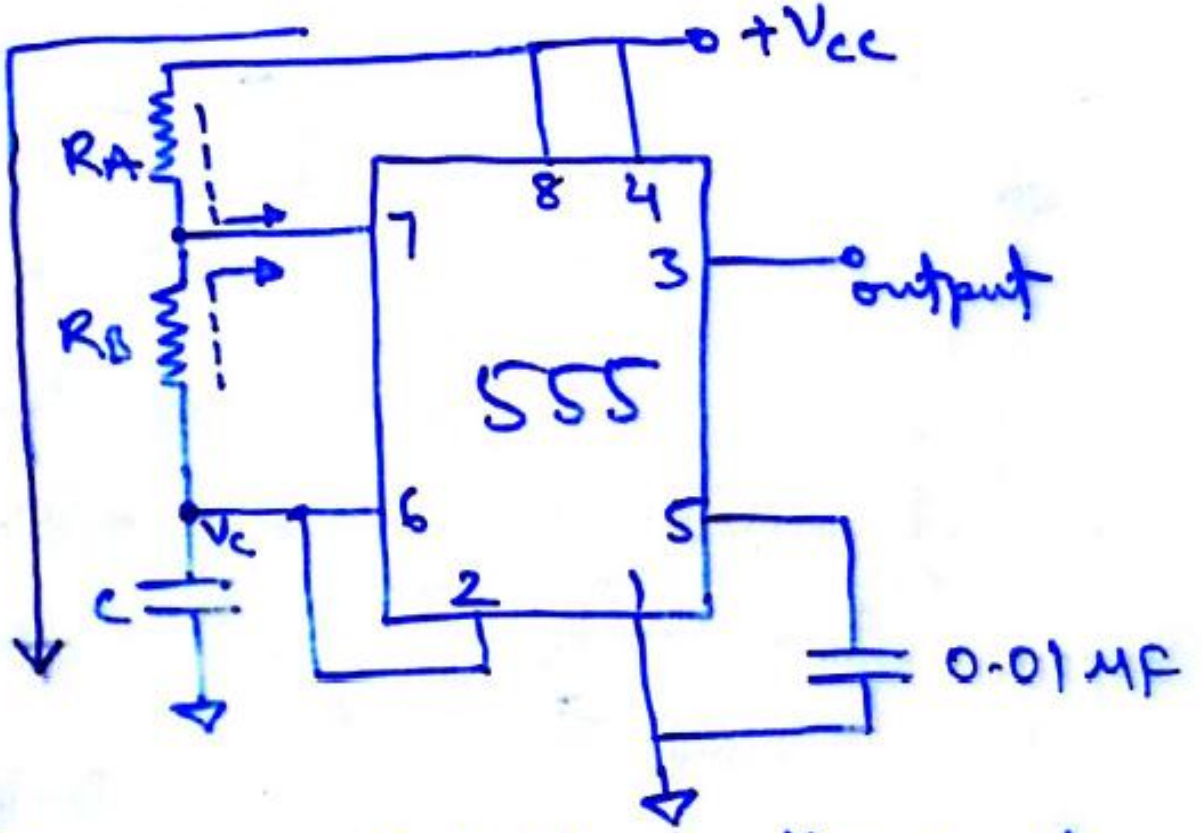


Fig 8-15. Astable multivibrator using 555 timer

Astable Operation cntd..

- For better understanding the complete diagram of Astable multivibrator with detailed internal diagram of 555 is shown in Figure 8.16.

Astable Operation cntd..

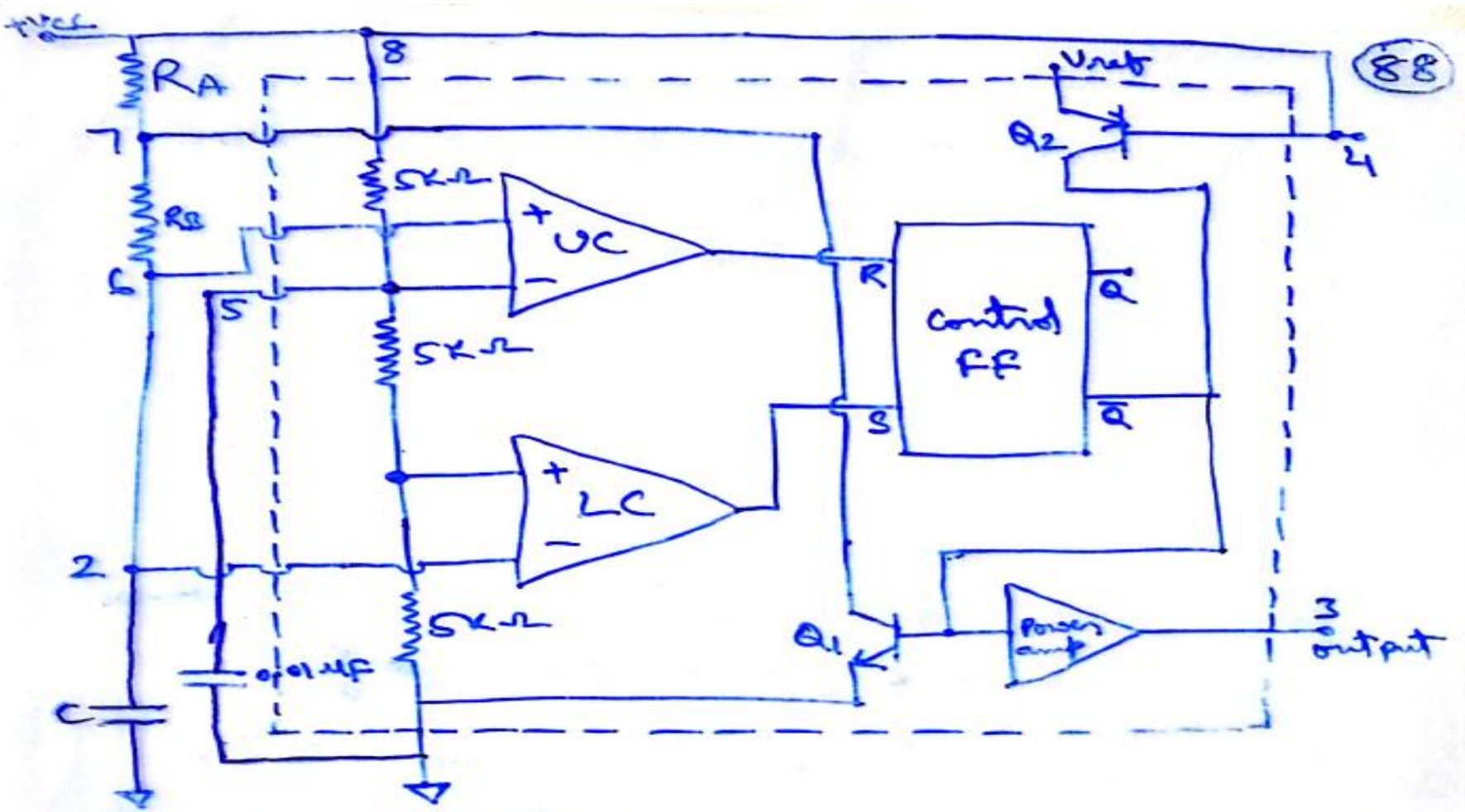


Fig 8-16 Functional diagram of Astable multivibrator using 555 timer.

Astable Operation cntd..

- Comparing with the monostable operation, the timing resistor is now split into two sections Ra and Rb. Pin 7 of discharging transistor Q1 is connected to the junction of Ra and Rb.
- When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc with a time constant (Ra+Rb)C. During this time, output(pin 3) is HIGH (equals Vcc) as RESET R=0, SET S=1 and this combination makes $\overline{Q}$=0 which has unclamped the timing capacitor C.

Astable Operation cntd..

- When the capacitor voltage equals 2/3 Vcc the upper comparator triggers the control FF so that $\overline{Q}$=1. This, in turn, makes the transistor Q1 on and capacitor C starts discharging towards ground through Rb and transistor Q1 with a time constant Rb C.
- Current also flows into transistor Q1 through Ra.
- Resistors Ra and Rb must be large enough to limit this current and prevent damage to the discharge transistor Q1.
- The minimum value of Ra is approximately equal to Vcc/0.2 where 0.2 A is the maximum current through the ON transistor Q1.

Astable Operation cntd..

- During the discharge of the timing capacitor C, as it reaches Vcc/3, the lower comparator is triggered and at this stage S=1, R=0, which turns Q=0. Now $\overline{Q}$=0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 Vcc and 1/3 Vcc respectively.
- Figure 8.17 shows the timing sequence and capacitor voltage waveform.

Astable Operation cntd..

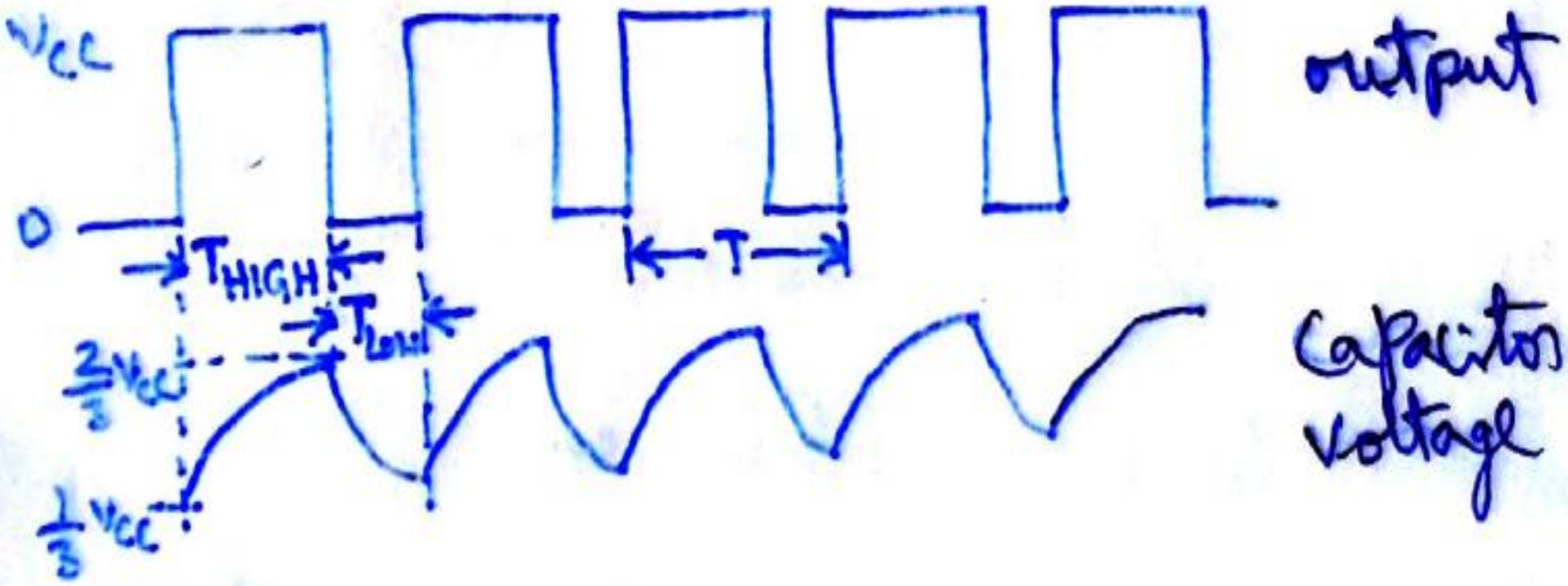


Fig 8.17 Timing Sequence of Astable multivibrator.

Astable Operation cntd..

- The length of Time that the output remains HIGH is the time for the capacitor to charge from 1/3 Vcc to 2/3 Vcc. It may be calculated as follows.
- The capacitor voltage for a low pass RC circuit subjected to a step input of Vcc volts is given by $V_c = V_{cc}(1 - e^{(-t/RC)})$
- The time t1 taken by the circuit to charge from 0 to 2/3 Vcc is

$$\frac{2}{3} V_{cc} = V_{cc}(1 - e^{(-t1/RC)}) \rightarrow t1 = 1.09\ RC$$

Astable Operation cntd..

And the time t2 to charge from 0 to 1/3 Vcc is

1/3 Vcc = Vcc (1- e^(-t2/RC)) ➔ t2 = 0.405 RC

So the time to charge from 1/3 Vcc to 2/3 Vcc

tHIGH = t1 –t2 = 1.09 RC – 0.405 RC = 0.69 RC

So, for the given circuit, tHIGH = 0.69 (Ra+Rb) C

The output is low while the capacitor discharges from 2/3 Vcc to 1/3 Vcc and the voltage across the capacitor is given by

1/3 Vcc =2/3 Vcc e^(-t/RC)

Astable Operation cntd..

Solving, we get $t = 0.69\ RC$

So for the given circuit, $t_{LOW} = 0.69\ R_b\ C$

Notice that both Ra & Rb are in the charge path, but only Rb is in the discharge path.

Therefore, Total time $T = t_{HIGH} + t_{LOW}$

$\rightarrow T = 0.69(R_a + 2R_b)\ C$

So $f = 1/T = 1.45/((R_a + 2R_b)\ C)$

Astable Operation cntd..

- The Duty cycle D of a circuit is defined as the ratio of ON time to the total time period

$$T = t_{ON} + t_{OFF}.$$

In this circuit, when the transistor Q1 is ON, the output goes LOW. Hence

$$D\ \% = (t_{LOW} / T) * 100$$

$$= Rb/(Ra + 2Rb) *100$$

With the circuit configuration of Fig 8.15 it is not possible to have a duty cycle more than 50% since tHIGH = 0.69 (Ra+Rb) C will always be greater than tLOW = 0.69 Rb C

Astable Operation cntd..

- In order to obtain a symmetrical square wave ie D =50%, the resistance Ra must be reduced to zero.
- However, now Pin 7 is connected directly to Vcc and extra current will flow through Q1 when it is ON. This may damage Q1 and hence the timer
- An alternate circuit which will allow duty cycle to be set at practically any level is shown in Figure 8.19.

Astable Operation cntd..

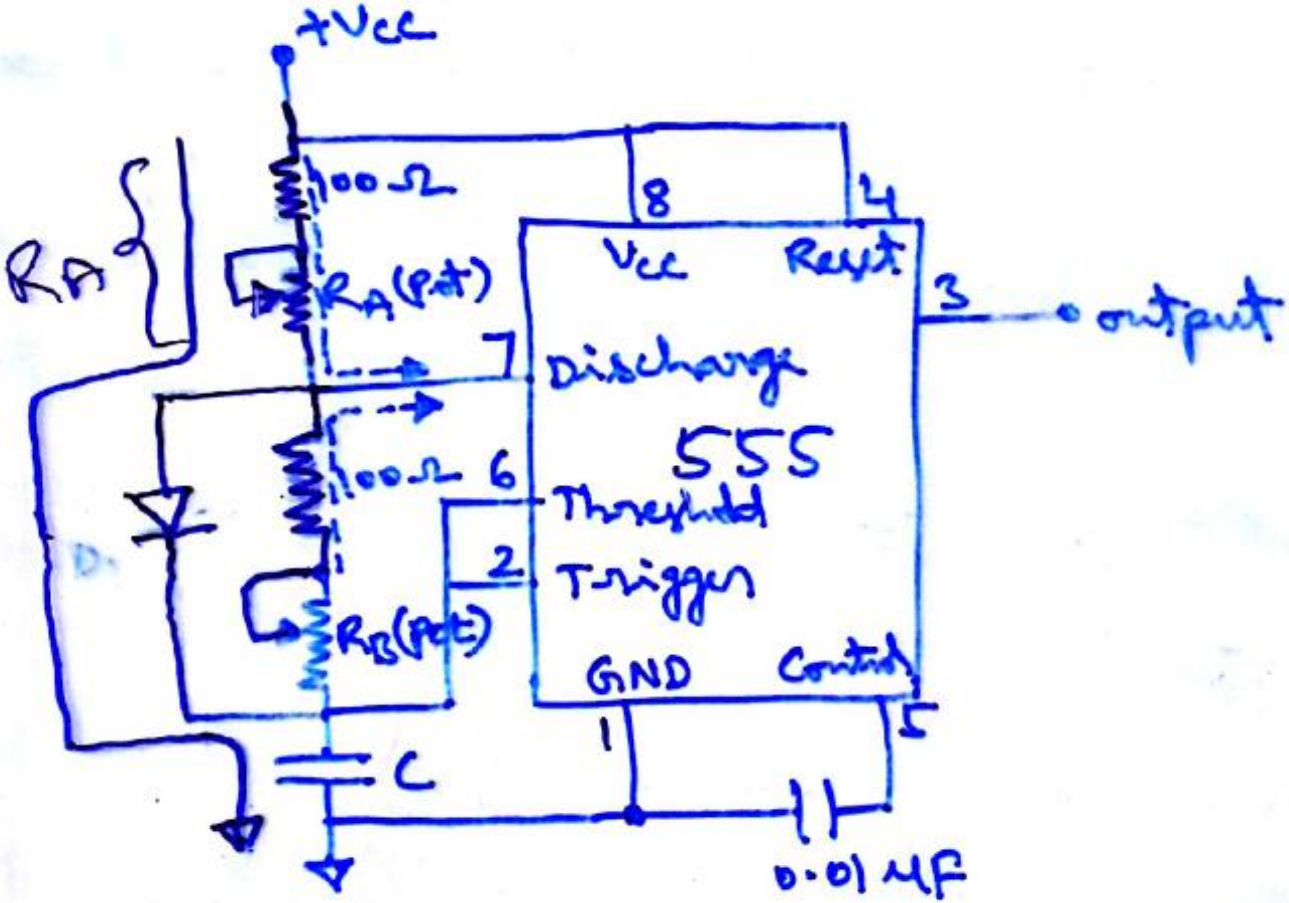


Fig 8.19 Adjustable duty cycle rectangular wave generator.

Astable Operation cntd..

- During the charging portion of the cycle, diode D1 is forward biased effectively short circuiting Rb so that tHIGH = 0.69 Ra C
- However, during the discharging portion of the cycle, transistor Q1 becomes ON, thereby grounding pin 7 and hence the diode D1 is reverse biased. So tLOW = 0.69 Rb C

Therefore T= tHIGH + tLOW = 0.69(Ra+Rb)C

➔ f = 1/T = 1.45 /(Ra+Rb)C

And Duty cycle, D = Rb /(Ra+Rb)

- Resistors Ra and Rb could be made variable to allow adjustment of frequency and pulse width.

Astable Operation cntd..

- However, a series resistor of at least 100Ω should be added to each Ra and Rb. This will limit peak current to the discharge transistor Q1 when the variable resistors are at minimum value.
- And, if Ra is made equal to Rb, then 50% duty cycle is achieved.

Astable Operation cntd..

Example: Refer Figure 8.15. For Ra = 6.8 KΩ, Rb = 3.3 KΩ and C=0.1 μF, calculate (a) tHIGH (b) tLOW (c) free running frequency (d) duty cycle D.

Astable Operation cntd..

Solution:

a) tHIGH = 0.69(Ra+Rb) C

= 0.69 (6.8 KΩ + 3.3 KΩ) 0.1 µF

= 0.7 ms

b) tLOW = 0.69 Rb C

= 0.69 (3.3KΩ) 0.1 µF

= 0.23 ms

Astable Operation cntd..

c) $f = 1.45/((Ra + 2Rb)\ C)$

$= 1.45/((6.8\ K\Omega + 2(3.3\ K\Omega))\ (0.1\ \mu F))$

$= 1.07\ KHz$

d) Duty Cycle $D = tLOW / T = Rb/(Ra + 2Rb)$

$= 3.3\ K\Omega /(6.8\ K\Omega + 2\ (3.3\ K\Omega))$

$= 0.25 = 25\%$

Applications in Astable Mode

- A couple of applications in Astable mode are
  - Pulse position modulator
  - FSK Generator

Pulse Position Modulator:

- The Pulse Position Modulator can be constructed by applying a modulating signal to pin5 of a 555 timer connected for Astable operation as shown in Figure 8.22.

Applications in Astable Mode cntd..

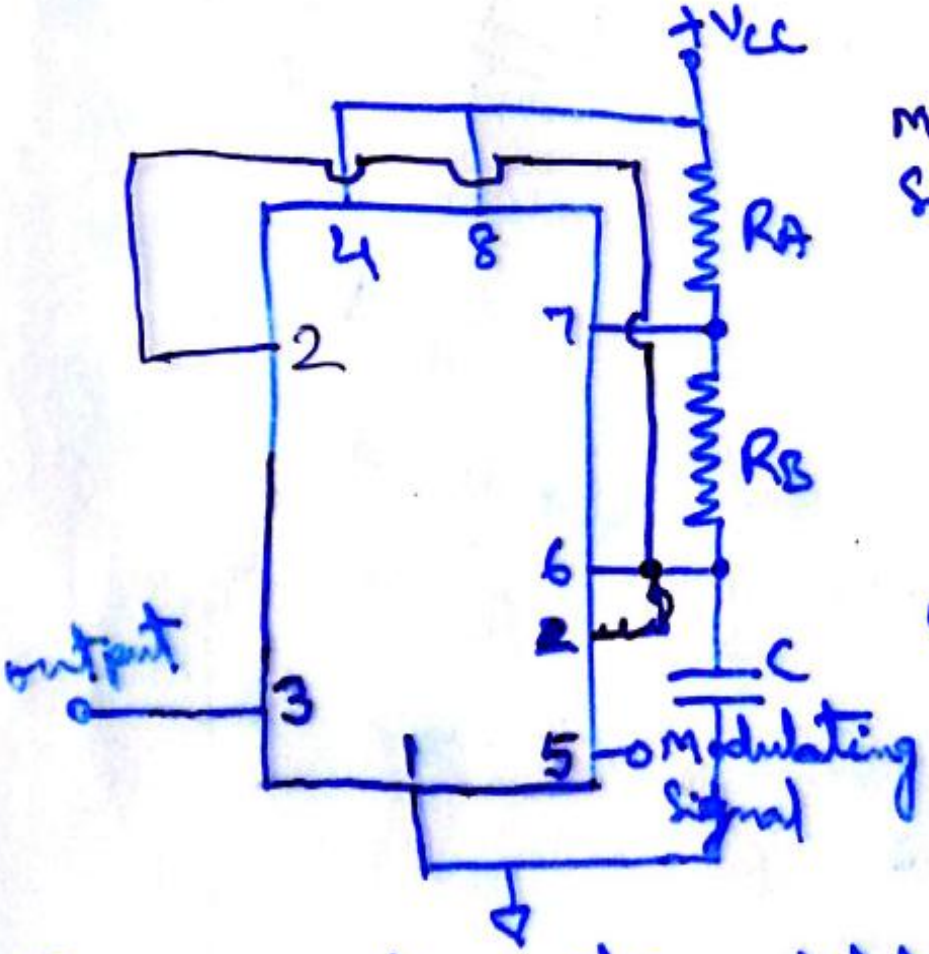


Fig 8-22 pulse position modulator

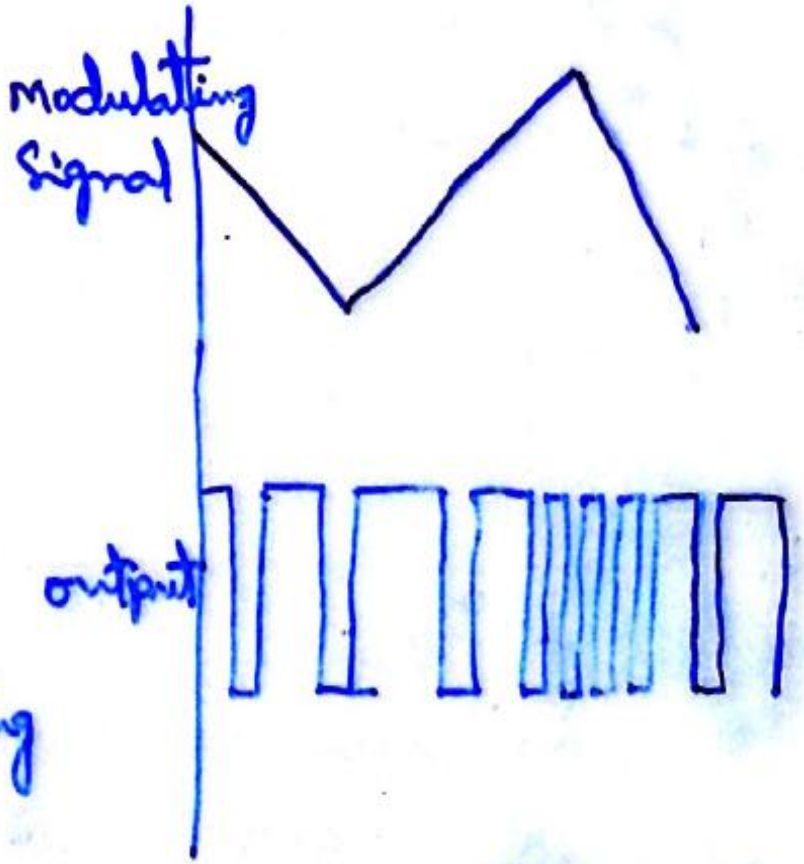


Fig 8-23 pulse position modulator output

Applications in Astable Mode cntd..

- The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.
- Figure 8.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation.

Phase Locked Loops: Introduction

- Although the evolution of the phase-locked loop began in the early 1930's, its cost outweighed it's advantages at first.
- With the rapid development of integrated circuit technology, however, the phase locked loop has emerged as one of the fundamental building blocks in electronics technology.
- The phase-locked loop principle has been used in applications such as FM stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, FSK decoders, and a generation of local oscillator frequencies and in TV and FM tuners.

Block Schematic and Operation Principle

- Figure 10.25 shows the phase-Locked loop (PLL) in its basic form.

Block Schematic and Operation Principle cntd..

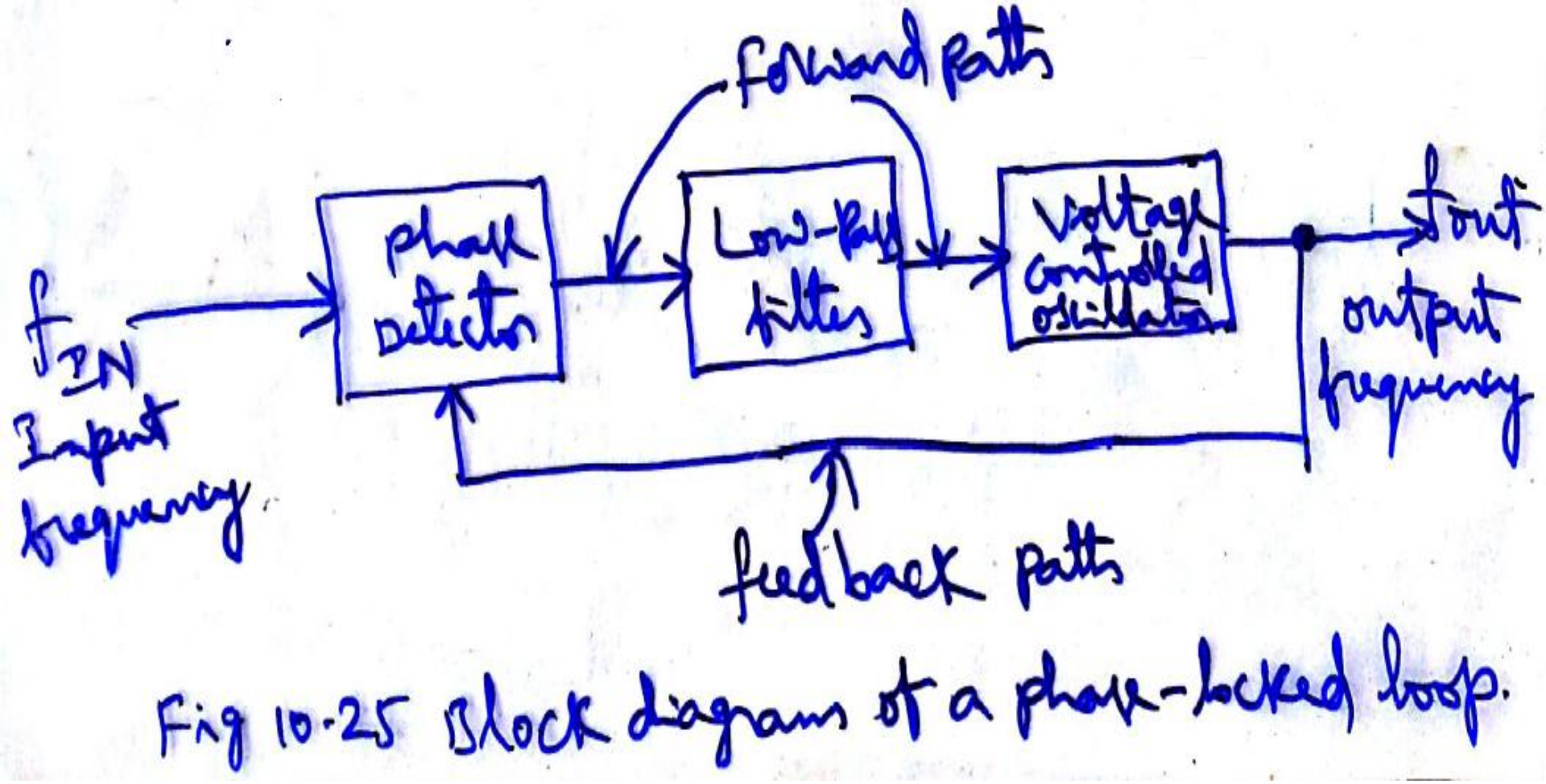


Fig 10-25 Block diagram of a phase-locked loop.

Block Schematic and Operation Principle cntd..

- As illustrated in this figure, the phase-locked loop consists of (1) a phase detector (2) a low-pass filter (3) a voltage controlled oscillator.
- The phase detector or comparator compares the input frequency fIN with the feed-back frequency fOUT. The output of the phase detector is proportional to the phase difference between fIN and fOUT. The output voltage of a phase detector is a DC voltage and therefore is often referred to as the error voltage.

Block Schematic and Operation Principle cntd..

- The output of the phase detector is then applied to the low pass filter, which removes the high frequency noise and produces a DC level. This DC level, in turn, is the input to the voltage controlled oscillator(VCO).
- The output frequency of the VCO is directly proportional to the input DC level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies.

Block Schematic and Operation Principle cntd..

- In short, the phase locked loop goes through three states: free-running, capture and phase lock.
- Before the input is applied, the phase locked loop is in the free-running state.
- Once the input frequency is applied, the VCO frequency starts to change and the phase locked loop is said to be in the capture mode.
- The VCO frequency continues to change until it equals the input frequency, and the phase-locked loop is then in the phase locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action.

Phase Detector

- The phase detector compares the input frequency and the VCO frequency and generates a DC voltage that is proportional to the phase difference between the two frequencies.
- Depending on the analog or digital phase detector used, the PLL is either called an analog or digital type respectively.
- A double balanced mixer is a classic example of an analog phase detector. On the other hand examples of digital phase detectors are these:

Phase Detector cntd..

1 Exclusive OR phase detector

2 Edge triggered phase detector

3 Monolithic phase detector

Exclusive OR Phase Detector:

- Figure 10.26a shows the exclusive OR phase detector that uses an exclusive OR gate such as CMOS type 4070.

Phase Detector cntd..

Inputs		output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = LOW
H = HIGH

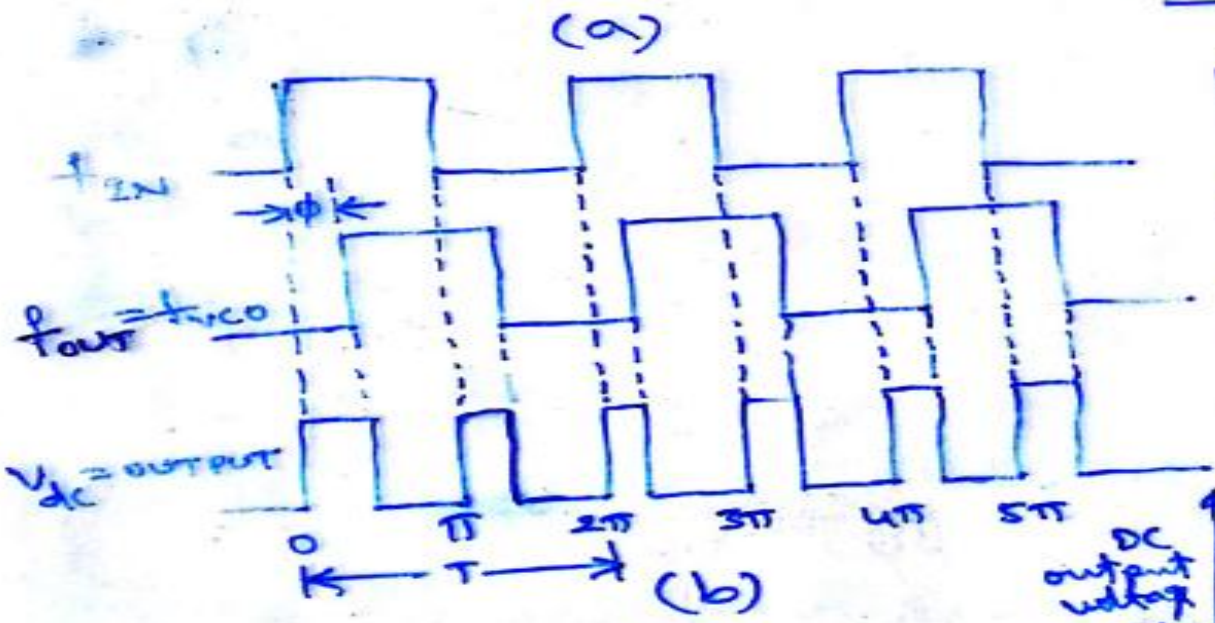
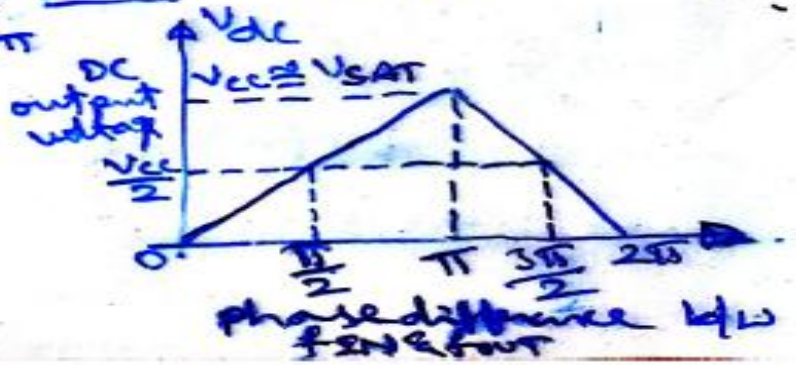


Fig 10-26 (a) Exclusive OR phase detector & logic diagram (b) I/P & O/P waveforms (c) Average O/P voltage vs phase difference b/w F_{IN} & f_{OUT}



Phase Detector cntd..

- The output of the exclusive OR gate is high only when fIN or fOUT is high, as shown in figure 10.26b.
- In this figure, fIN is leading fOUT by ϕ degrees

ie the phase difference between fIN and fOUT is ϕ degrees.

- The DC output voltage of the exclusive OR phase detector is a function of the phase difference between its two inputs.

Phase Detector cntd..

- Figure 10.26 c shows DC output voltage as a function of the phase difference between fIN and fOUT. This graph indicates that the maximum DC output voltage occurs when the phase difference is Π radians or 180 degrees.
- The slope of the curve between 0 and Π radians is the conversion gain Kp of the phase detector.

  For example, if the exclusive OR gate uses a supply voltage Vcc = 5 V, the conversion gain Kp is

  $$Kp = 5V/\Pi = 1.59 \text{ V/Radians}$$

Phase Detector cntd..

- The exclusive OR type of phase detector is generally used if fIN and fOUT are square waves.
- The edge triggered phase detector, on the other hand, is preferred if the fIN and fOUT are pulse waveforms with less than 50% duty cycles.
- These both types of phase detectors are sensitive to harmonics of the input signal and changes in duty cycles of fIN and fOUT. In such cases Monolithic phase detector is used

Low Pass Filter

- The second block shown in the PLL block diagram of figure 10.25 is a low-pass filter.
- The function of the low-pass filter is to remove the high frequency components in the output of the phase detector and to remove high frequency noise.
- More important, the low-pass filter controls the dynamic characteristics of the phase-locked loop. These characteristics include capture and lock ranges, band width, and transient response.

Low Pass Filter cntd..

- The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN. An equivalent term for lock range is the tracking range.
- On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously the capture range is always smaller than the lock range.

Low Pass Filter cntd..

- As the filter bandwidth is reduced, it's response time increases. However, reduced band width reduces the capture range of PLL.
- Nevertheless, reduced bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes the noise
- The loop filter used in the PLL may be one of the three types shown in figure 10.29.

Low Pass Filter cntd..

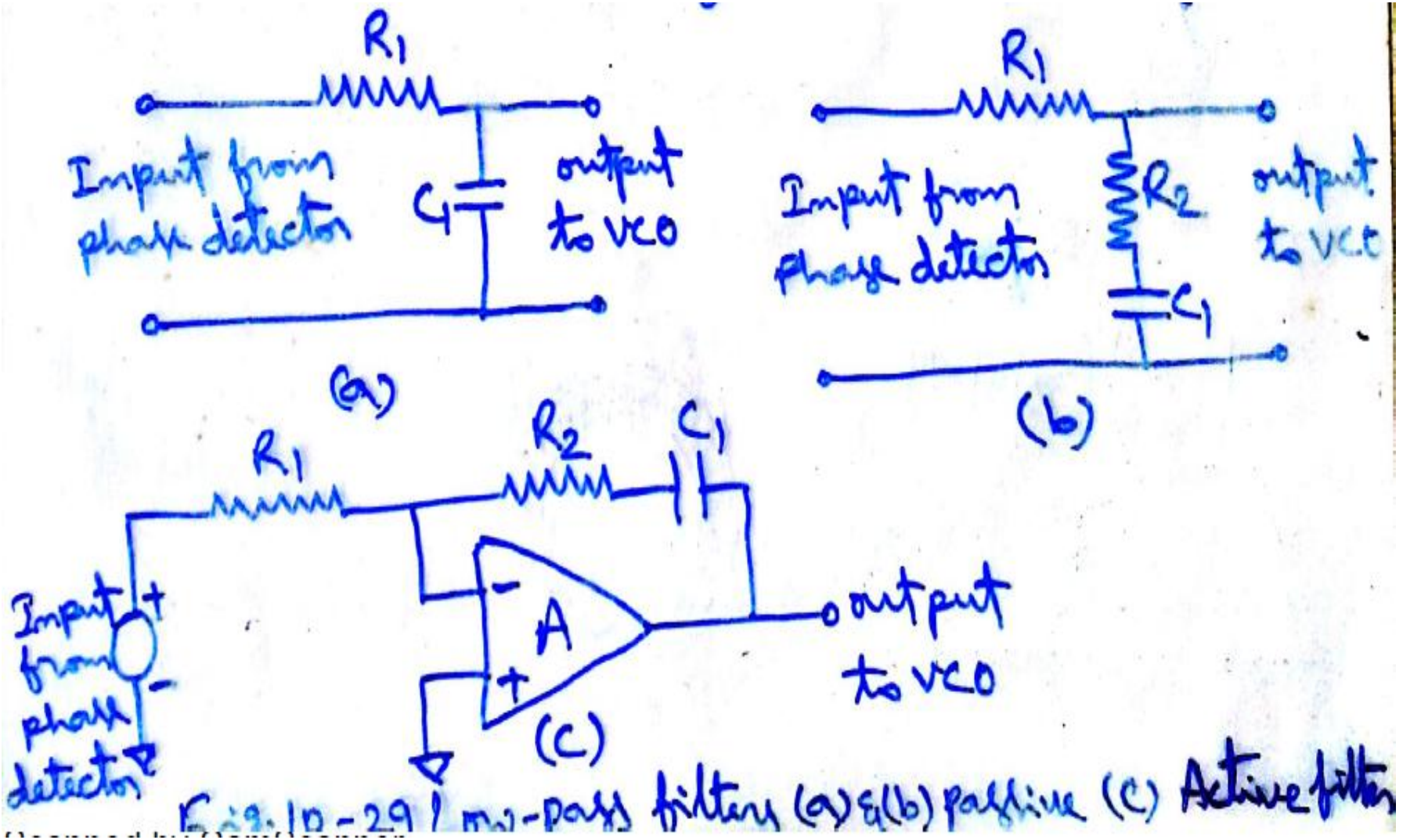


Fig 3.10-29 Low-pass filters (a) & (b) passive (c) Active filter

Low Pass Filter cntd..

- With the passive filters of Figure 10.29a and b, an amplifier is generally used for gain. On the other hand, the active filter of Figure 10.29c includes the gain.

Voltage Controlled Oscillator

- A third section of the PLL is the voltage controlled oscillator.
- The VCO generates an output frequency that is directly proportional to it’s input voltage. The block diagram of the VCO is shown in Figure 10.30.

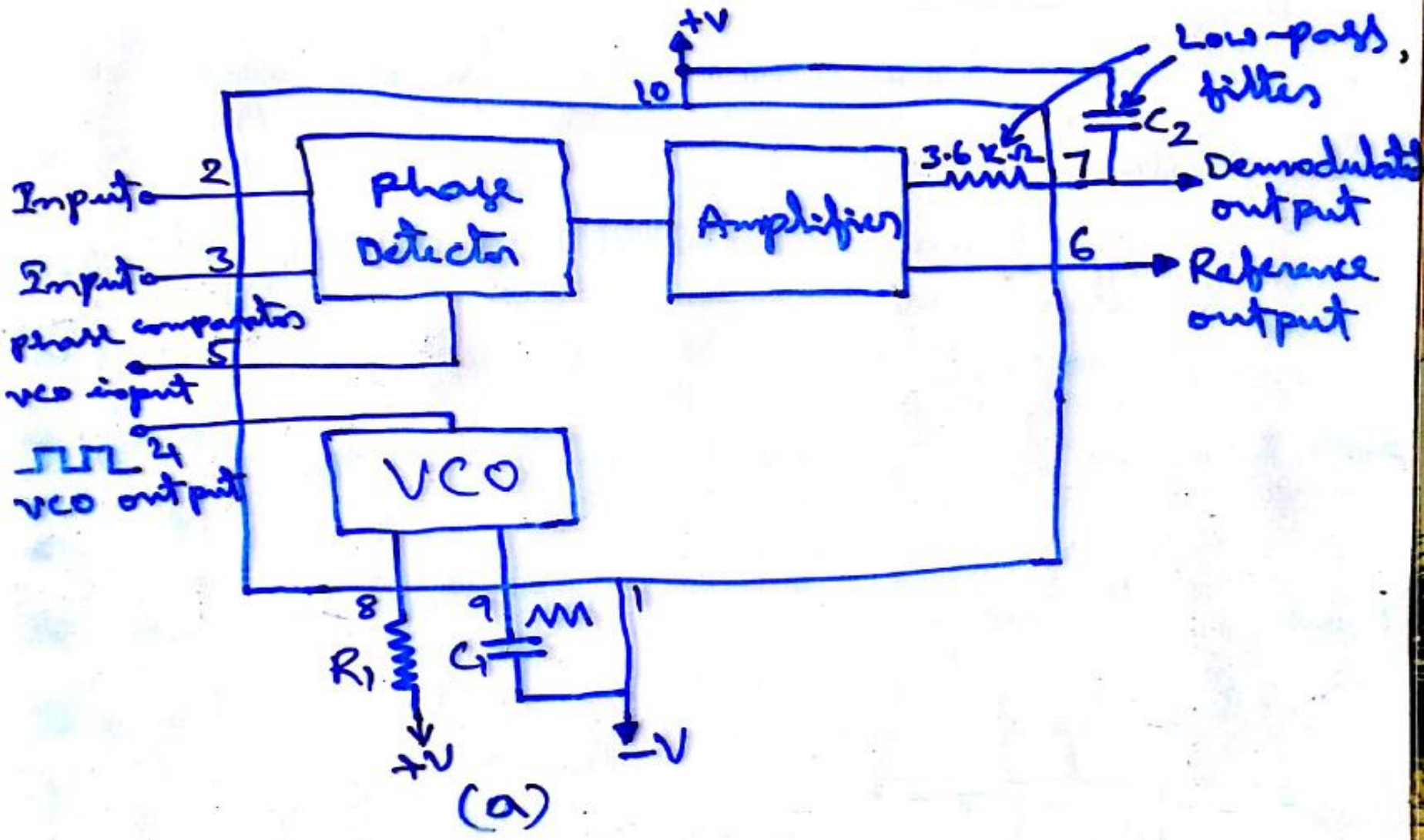
Voltage Controlled Oscillator cntd..

Fig 10-30 VCO Block diagram.

565 PLL

- Figure 10.32 shows the block diagram and connection diagram of the 565 PLL. The device is available as a 14 pin DIP package and as 10 pin metal can package.

565 PLL cntd..


+V
10
Low-pass filter
C_2
3.6 kΩ
7
Demodulated output
6
Reference output
Input
2
Input
3
Phase Detector
Amplifier
phase comparator
5
VCO input
4
VCO output
VCO
8
9
1
R_1
C_1
+V
−V
(a)

565 PLL cntd..

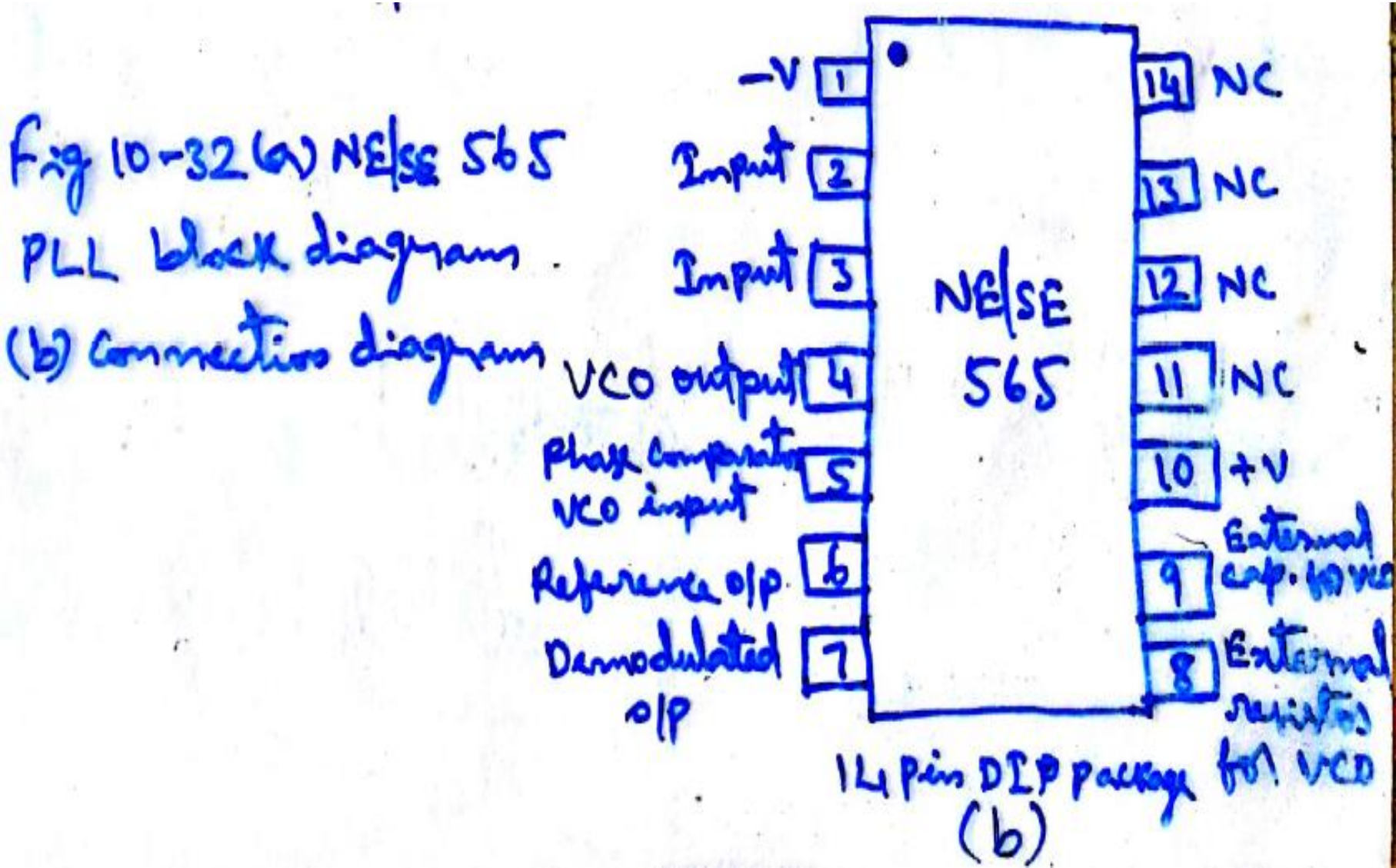


Fig 10-32 (a) NE/SE 565 PLL block diagram (b) Connection diagram
-V
Input
Input
VCO output
Phase comparator VCO input
Reference o/p
Demodulated o/p
NE/SE 565
NC
NC
NC
NC
+V
External cap. for VCO
External resistors for VCO
14 pin DIP package
(b)

565 PLL cntd..

- The central frequency of the PLL is determined by the free running frequency of the VCO, which is given by the equation

  $$f_{OUT} = 1.2/(4\ R1\ C1)\ \text{Hz}$$

  where R1 and C1 are external resistor and capacitor connected to pins 8 & 9 respectively.
- The VCO free running frequency fOUT is adjusted externally with R1 and C1 to be at the center of the input frequency range.
- Although C1 can be any value, R1 must have a value between 2 KΩ and 20 KΩ

565 PLL cntd..

- A capacitor C2 connected between pin 7 and positive supply (pin 10) forms a first order low-pass filter with an internal resistance of 3.6 KΩ.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage at Pin 7 in order to stabilize the VCO frequency.
- The 565 PLL can lock to and track an input signal over typically + or – 60% bandwidth with respect to fOUT as the center frequency.
- The lock range fL and capture range fC of the PLL are given by the following equations:

565 PLL cntd..

fL = + or – 8 fOUT/ V Hz

Where fOUT=free running frequency of VCO (Hz)

V = v – (-v) volts

and fC = + or – [fL/((2π) (3.6 * 10^3) C2)]^(1/2)

Where C2 is in Farads.

- The lock range usually increases with an increase in input voltage but decreases with an increase in supply voltages.

565 PLL cntd..

- Pins 2 & 3 are the input terminals and an input signal can be direct-coupled, provided that there is no DC voltage difference between the pins and DC resistances seen from pins 2 & 3 are equal.
- A short between pins 4 & 5 connects the VCO output (fOUT) to the phase comparator and enables the comparator to compare fOUT with the input signal fIN.

Applications of PLL

Frequency Multiplication:

- Figure 9.12 gives the block diagram of a frequency multiplier using PLL.

Frequency Multiplication

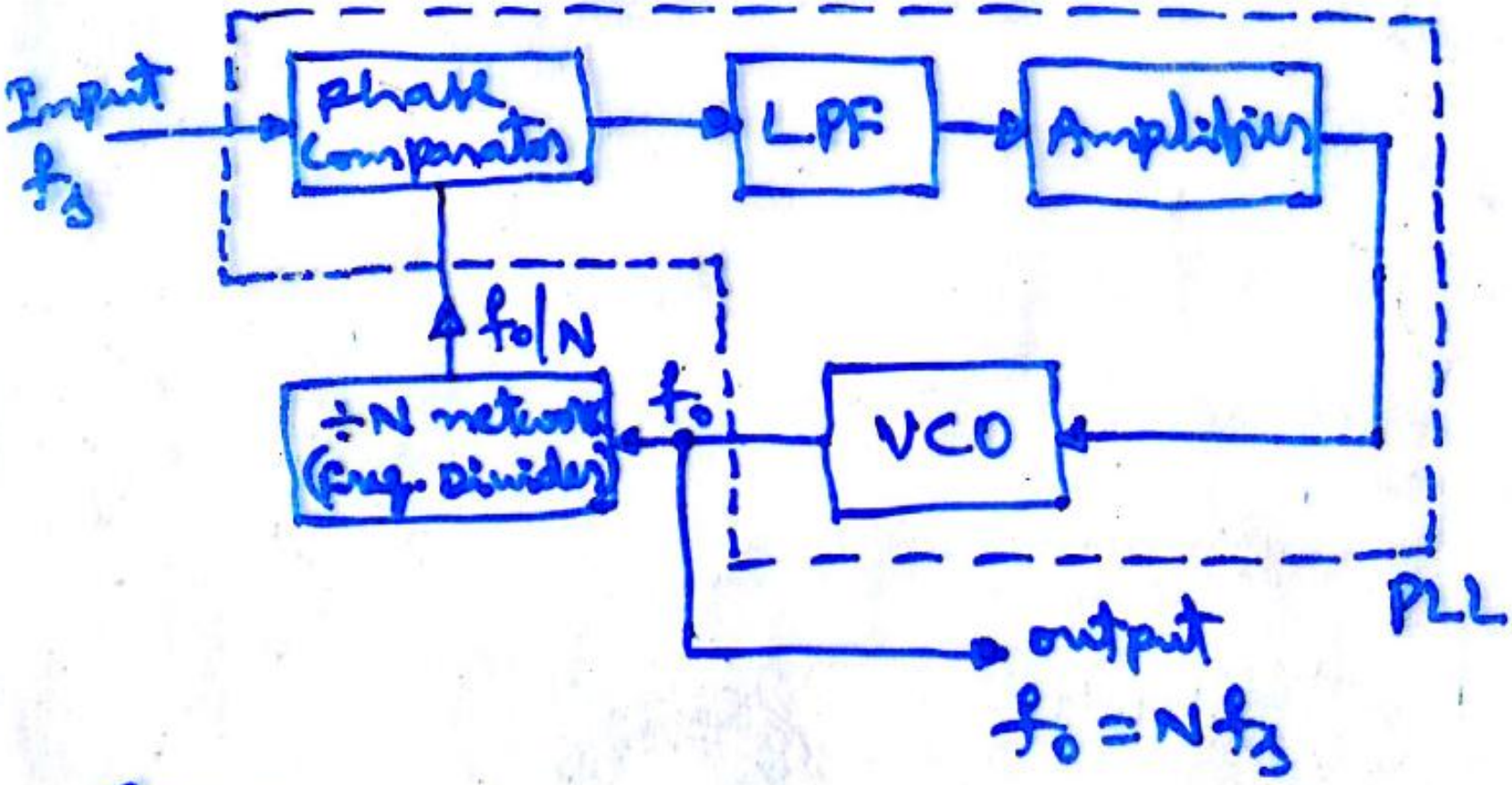


Fig 9.12 Frequency multiplier using IC PLL

Frequency Multiplication cntd..

- A divide by N network is inserted between the VCO output and the phase comparator input.
- In the locked state, the VCO output frequency fo is given by

$$f_o = Nf_s$$

- The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

End of Unit II

Unit III

Data Converters

Introduction

- Most of the real world physical quantities such as voltage, current, temperature, pressure and time etc are available in analog form.
- Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store, or transmit the analog signal with out introducing considerable error because of superimposition of noise as in the case of amplitude modulation.
- Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise.

Introduction cntd..

- The operation of any digital communication system is based upon Analog to Digital (A/D) and Digital to Analog (D/A) convertion.
- Figure 10.1, highlights a typical application with in which A/D and D/A conversion is used.

Introduction cntd..

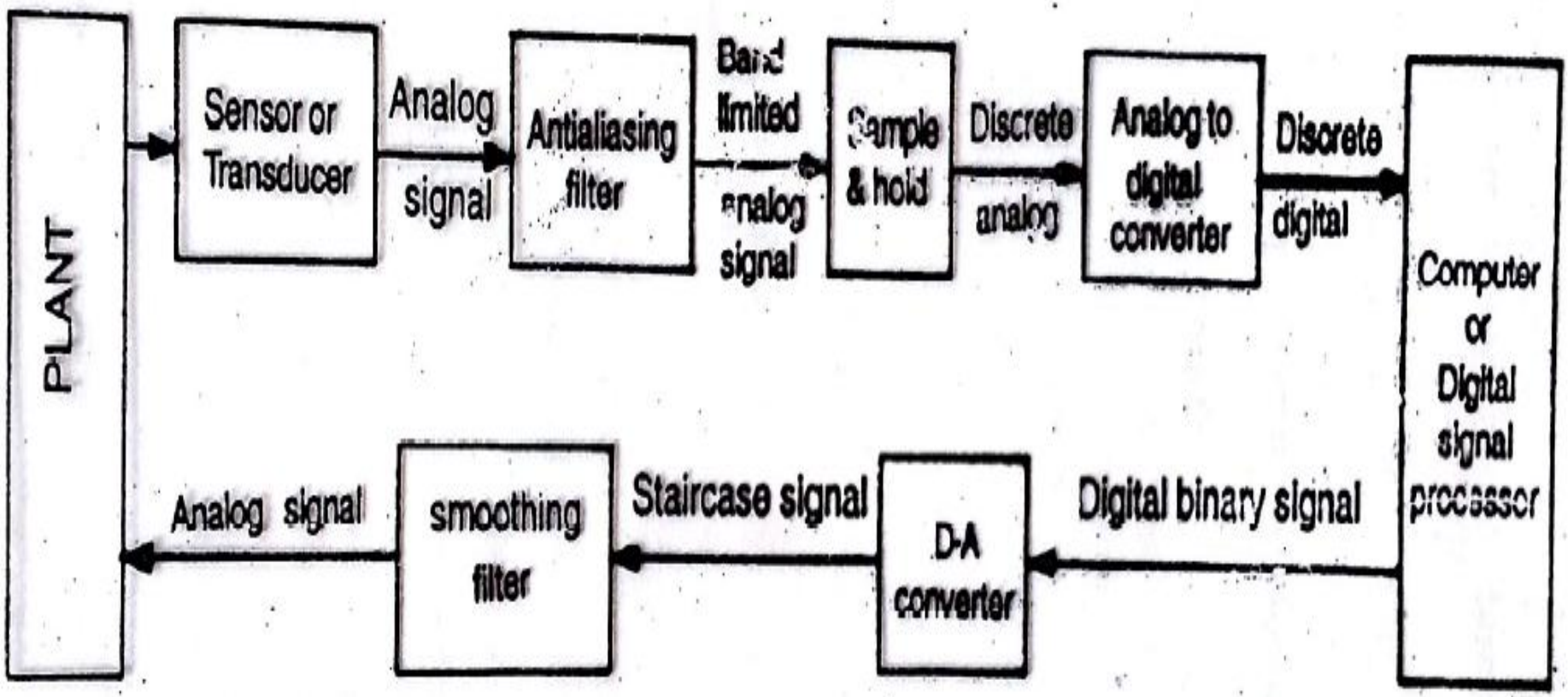


Fig. 10.1 Circuit showing application of A/D and D/A converter

Introduction cntd..

- The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or Digital signal processor performs the numerical calculations of the desired control algorithm.

Introduction cntd..

- The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC.
- The output of a D/A converter is commonly a staircase. This staircase like output is passed through a smoothing filter to reduce the effect of quantization noise.

Applications of A/D and D/A conversion

- The scheme given in Figure 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multi meter, direct digital control, digital signal processing, microprocessor based instrumentation.

Basic DAC techniques

- The schematic of a DAC is shown in Figure 10.2.

Basic DAC techniques cntd..

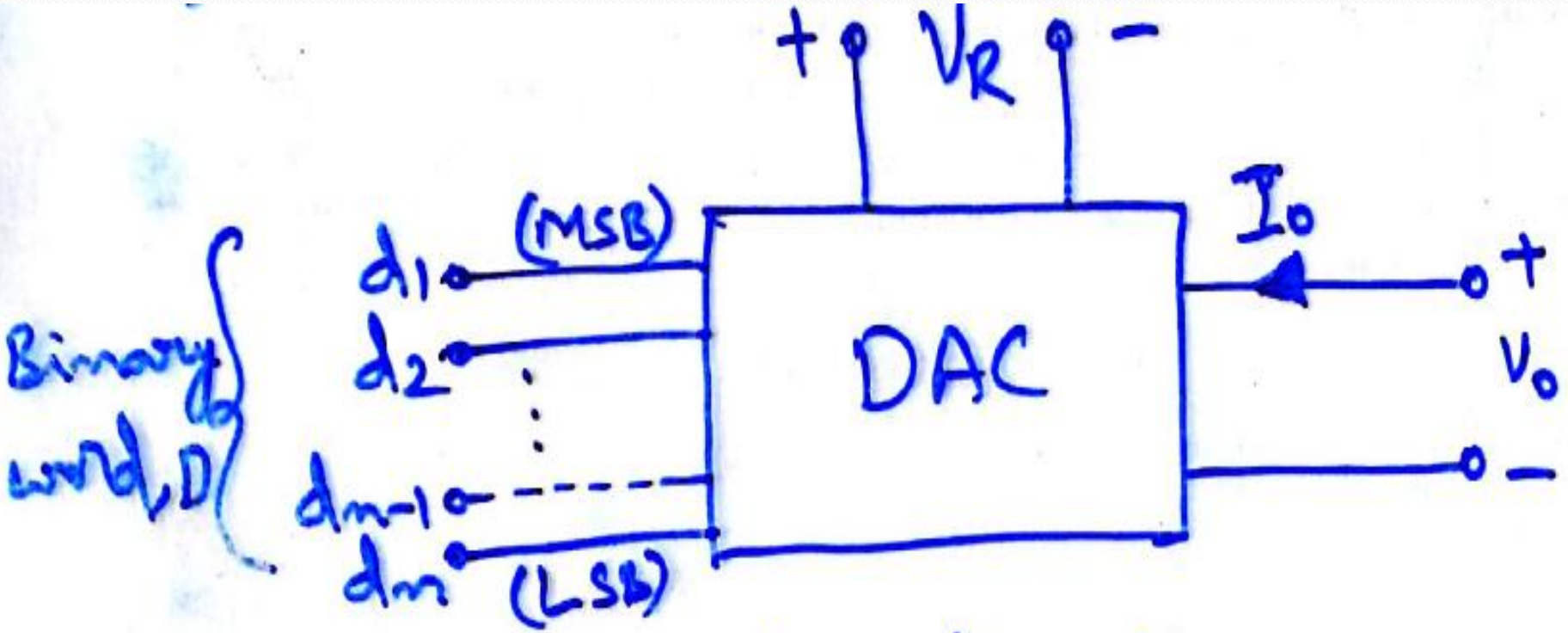


Fig 10.2 Schematic of a DAC

Basic DAC techniques cntd..

- The input is an n-bit binary word D and is combined with a reference voltage vR to give an analog output signal.
- The output of a DAC can be either a voltage or current.
- For a voltage output DAC, the D/A converter is mathematically described as

$V_0 = K V_{fs}(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \text{-----} + d_n 2^{-n})$----(1)

Where V_0 = output voltage, V_{fs}=full scale output voltage

K = scaling factor usually adjusted to unity

d_1 d_2 d_3 ------- d_n = n-bit binary fractional word

d_1 = MSB with weight of $V_{fs}/2$,
d_n =LSB with a weight of $V_{fs}/2^n$

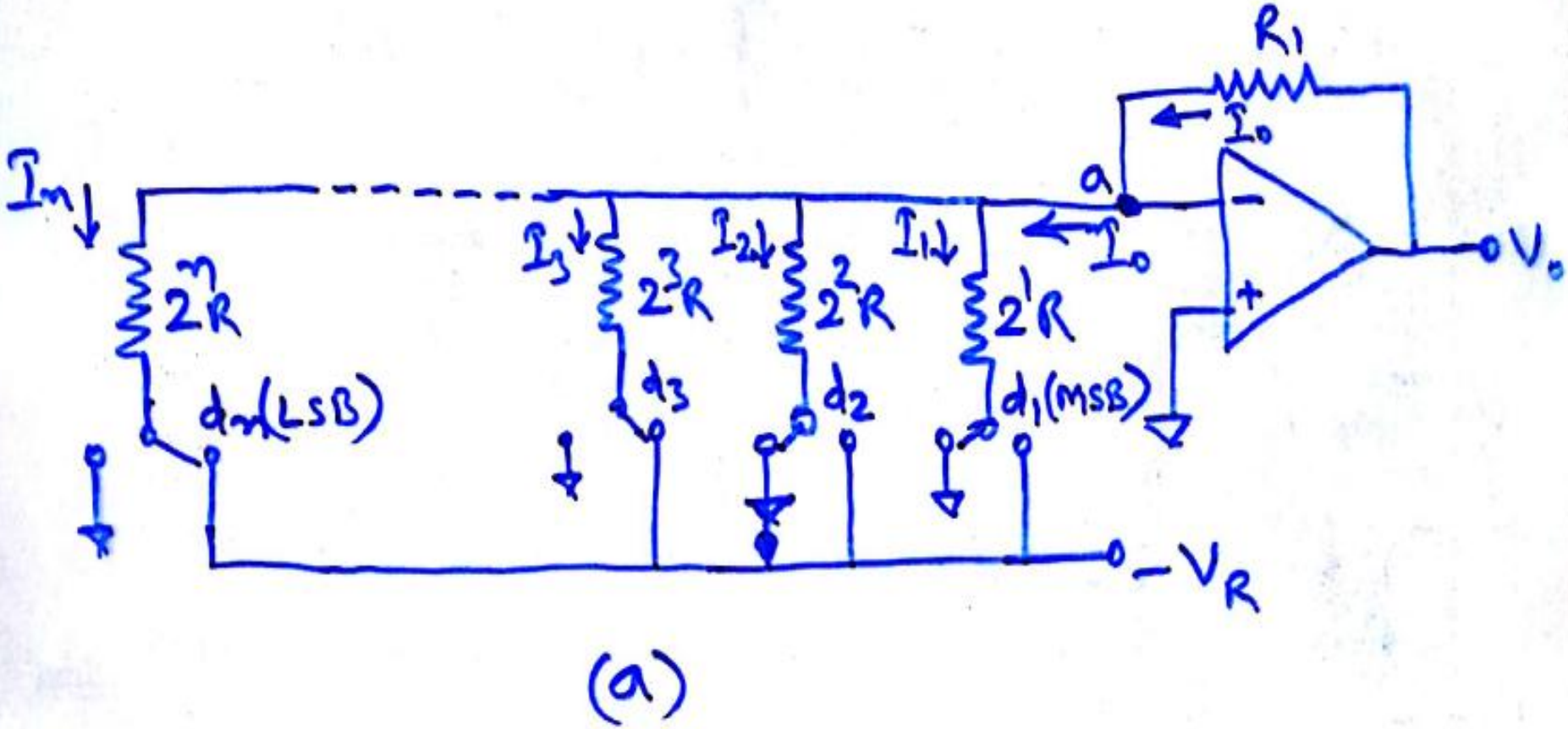
Basic DAC techniques cntd..

- There are various ways to implement eq(1). Here we shall discuss the following resistive techniques only
  - Weighted resistor DAC
  - R-2R Ladder DAC
  - Inverted R-2R Ladder DAC

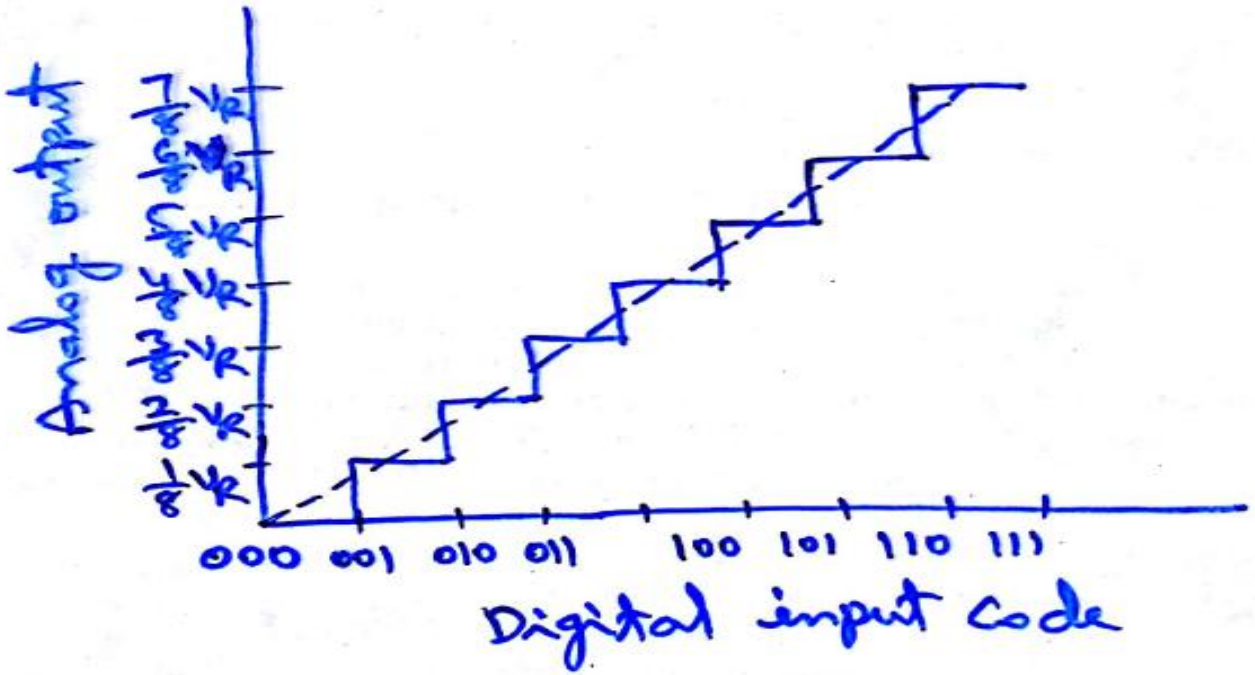
Weighted Resistor DAC:

- One of the simplest circuits shown in Figure 10.3a uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches d1, d2, d3, ---- dn, controlled by Binary input word.

Weighted Resistor DAC cntd..



Weighted Resistor DAC cntd..



(b)

Fig 10.3 (a) A simple weighted resistor DAC
(b) Transfer characteristics of a 3-bit DAC.

Weighted Resistor DAC cntd..

- These switches are single pole double throw (SPDT) type.
- If the Binary input to a particular switch is 1, it connects the resistance to the reference voltage (-Vr). And if the input bit is zero, the switch connects the resistor to ground.
- From Figure 10.3a, the output current Io for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \text{----------} + I_n$$

$$= (V_r/(2R))\, d_1 + (V_r/(2^2 R))\, d_2 + \text{-----} + (V_r/(2^n R))\, d_n$$

$$= V_r/R\,(d_1\, 2^{-1} + d_2\, 2^{-2} + \text{---------} + d_n\, 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_r R_f/R\,(d_1\, 2^{-1} + d_2\, 2^{-2} + \text{----} + d_n\, 2^{-n}) - (2)$$

Weighted Resistor DAC cntd..

- Comparing eq(1) with eq(2), we get

  if Rf = R, then K=1, and Vfs = Vr

- The circuit shown in Figure 10.3a uses a –ve reference voltage. The analog output voltage is therefore +ve staircase as shown in Figure 10.3b for a 3-bit weighted resistor DAC.
- It may be noted that
  - Although the op-amp in Figure 10.3a is connected in inverting mode, it can also be connected in non-inverting mode.

Weighted Resistor DAC cntd..

- The op-amp is simply working as a current-to-voltage converter.
- The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches , the reference voltage should be +5V and the output will be –ve.

Problems with Weighted Resistor DAC

- The accuracy and stability of a DAC depends up on the accuracy of the resistors and tracking of each other with temperature.
- There are, however, a number of problems associated with this type of DAC.
- One of the disadvantages of Binary weighted resistor type DAC is the wide range of resistor values required.
- It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bits increases, the range of resistance value increases.

Problems with Weighted Resistor DAC cntd..

- For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, ------, 2^8 R. The largest resistor is 128 times the smallest one for only 8-bit DAC.
- For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5KΩ.
- The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy.
- The choice of smallest resistor value as 2.5 KΩ is reasonable, otherwise loading effect will be there.

Problems with Weighted Resistor DAC cntd..

- The difficult of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8 bits.

R-2R Ladder DAC:

- Wide range of resistors are required in Binary Weighted Resistor type DAC. This can be avoided by using R-2R Ladder type DAC where only two values of resistors are required.
- It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 KΩ to 10KΩ.

R-2R Ladder type DAC cntd..

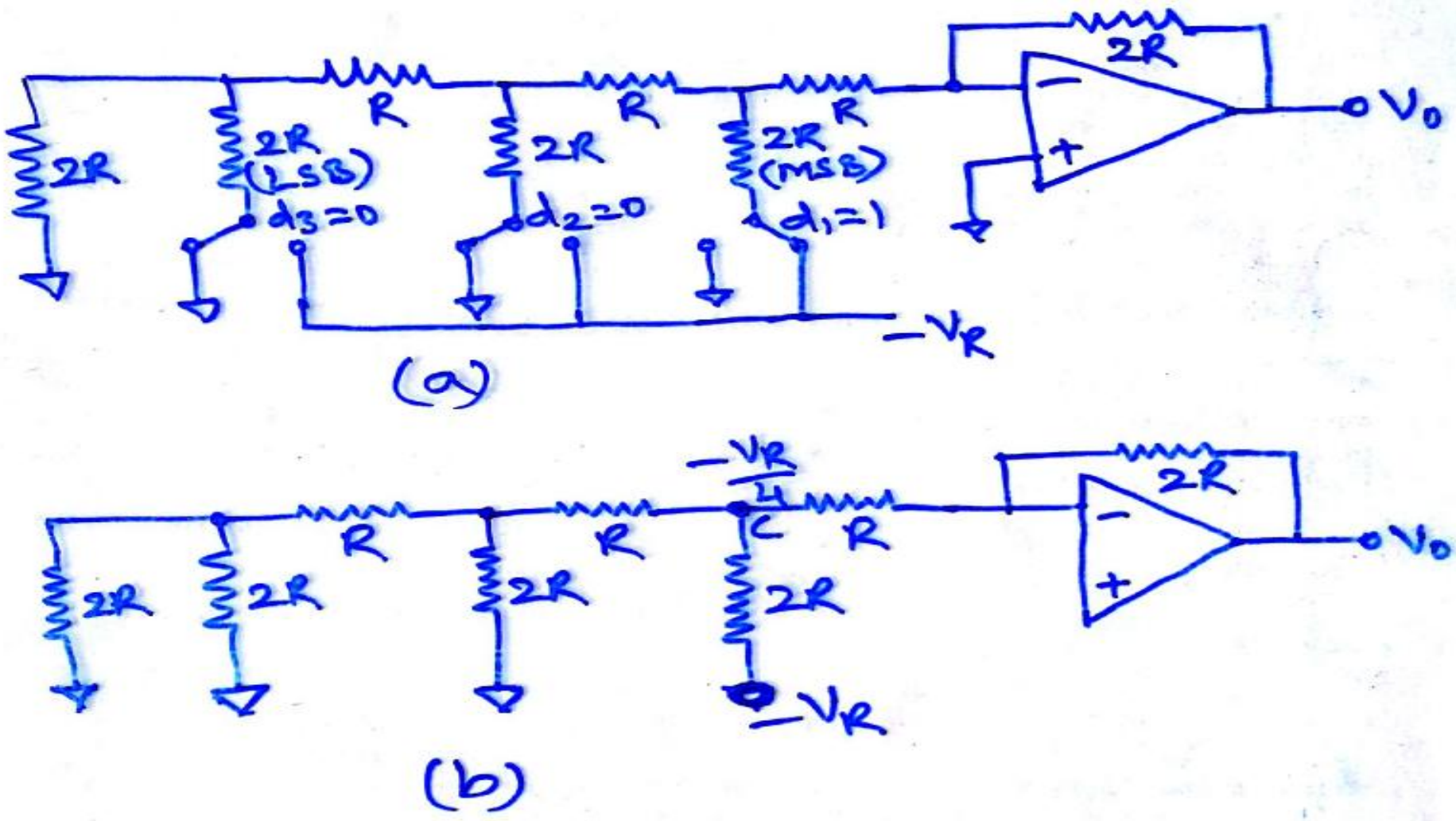
- For simplicity, consider a 3-bit DAC as shown in Figure 10.5a, where the switch position d1 d2 d3 corresponds to the Binary word 100.
- The circuit can be simplified to the equation form of Figure 10.5b and finally to Figure 10.5c.
- Then, voltage at node C can be easily calculated by the set procedure of network analysis as

  $-Vr\ ((2/3)\ R)\ /\ (2R + (2/3)R) = -Vr/4$

- The output voltage

  $Vo = -2R/R(-Vr/4) = Vr/2 = Vfs/2$

R-2R Ladder type DAC cntd..



R-2R Ladder type DAC cntd..

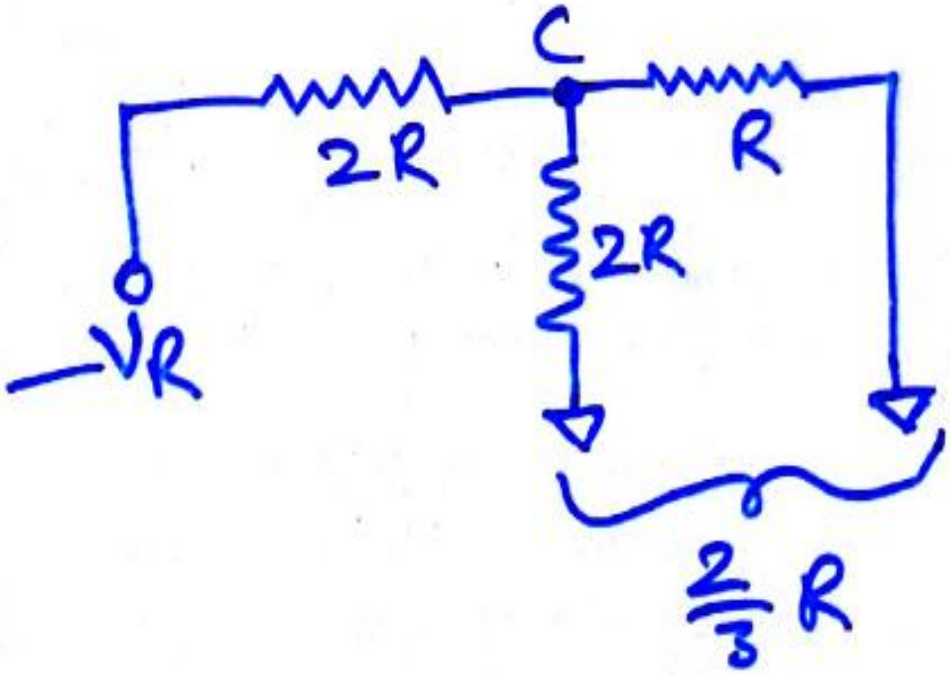


Fig 10-5(a) R-2R ladder DAC (b) Eq. ckt of (a)
(c) eq. ckt of (b).

A/D Converters

- The block schematic of ADC shown in Figure 10.9 provides the function just opposite to that of a DAC.

A/D Converters cntd..

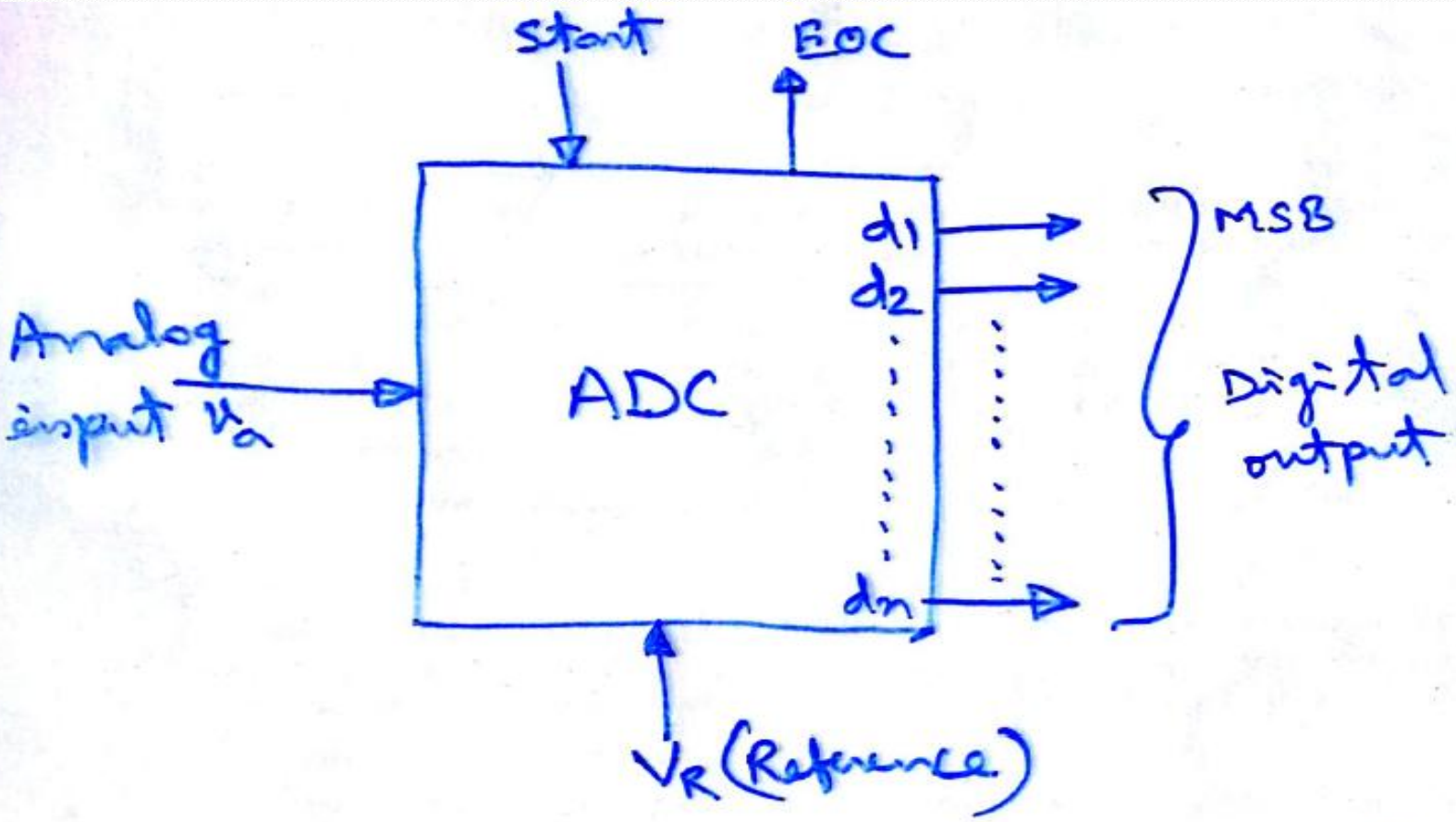


Fig 10.9 Functional diagram of ADC.

A/D Converters cntd..

- It accepts an analog input voltage Va and produces an output binary word d1d2--------dn of functional value D, so that

D = d1 2^-1 + d2 2^-2 + ---------- + dn 2^-n

where d1 is the MSB and dn is the LSB.

- An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and EOC (end of conversion) output to announce when the conversion is complete.
- Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

A/D Converters cntd..

- ADCs are classified broadly into two groups according to their conversion technique
  - Direct type ADCs
  - Integrating type ADCs
- Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes
  - Flash (comparator) type converter
  - Counter type converter
  - Tracking or servo conveter
  - Successive approximation type converter
- Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

A/D Converters cntd..

- Charge balancing ADC
- Dual slope ADC

Successive Approximation Converter

- The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods.
- For example, an 8-bit converter would require eight clock pulses to obtain a digital output. Figure 10.13 shows an 8-bit converter.

Successive Approximation Converter cntd..

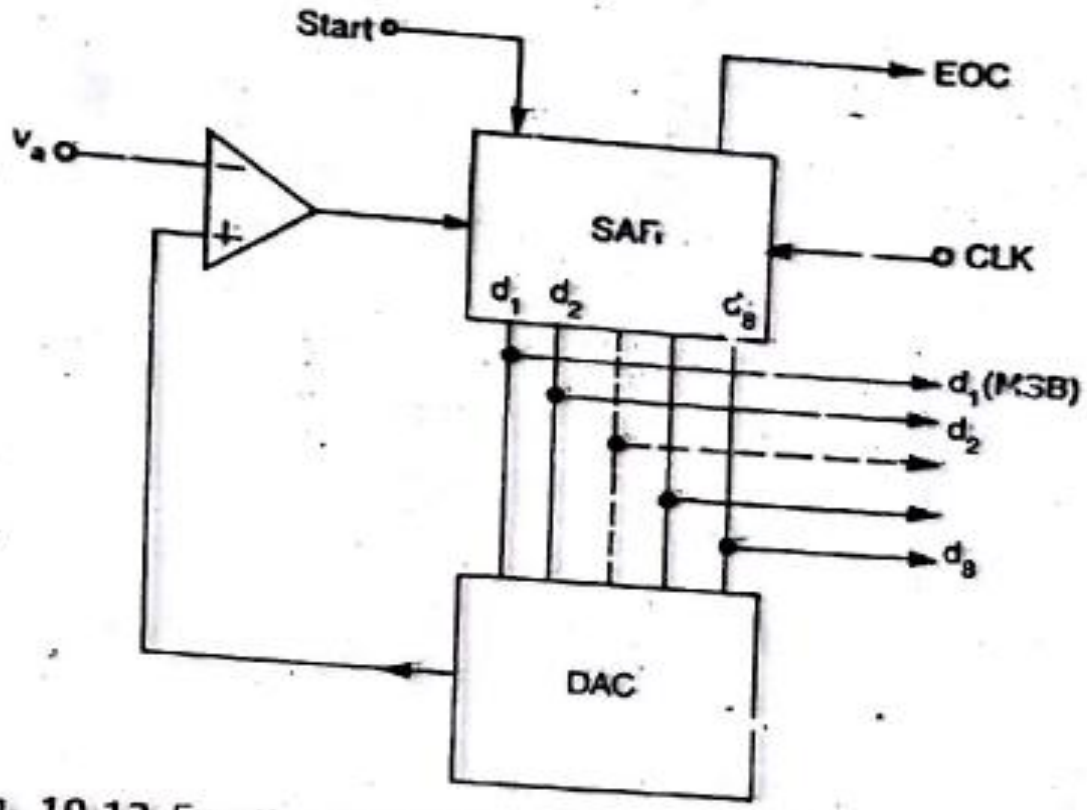


Fig. 10.13 Functional diagram of the successive approximation ADC

Successive Approximation Converter cntd..

- The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

Circuit Operation:

- With the arrival of the START command the SAR sets the MSB d1=1, with all other bits to zero so that the trial code is 10000000.
- The output Vd of the DAC is now compared with analog input Va.
- If Va is greater than the DAC output Vd, then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

Successive Approximation Converter cntd..

- However, if Va is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to zero and go on to the next lower significant bit.
- This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.
- Whenever the DAC output crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command.
- Figure 10.14a shows a typical conversion sequence and Figure 10.14b shows the associated waveforms.

Successive Approximation Converter cntd..

Correct digital representation	Successive approximation register output V_a at different stages in the conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 10.14 (a) Successive approximation conversion sequence for a typical analog input

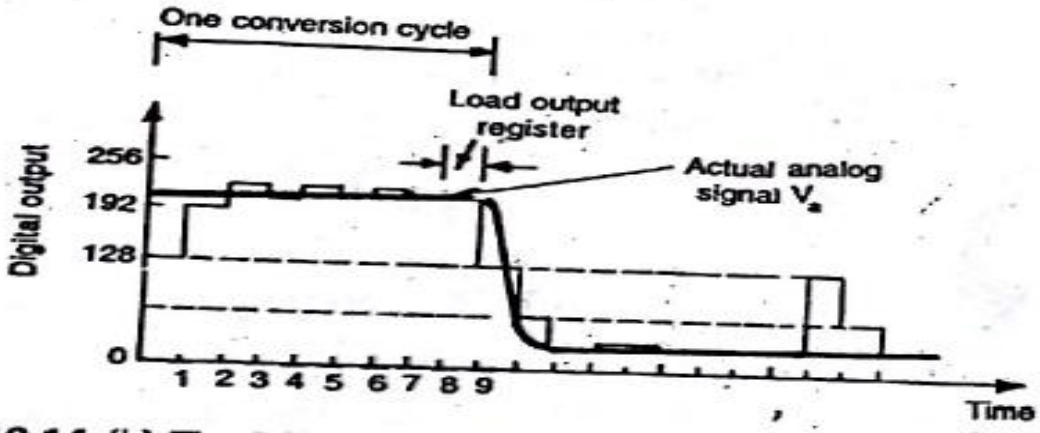


Fig. 10.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

Successive Approximation Converter cntd..

- It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage.
- It requires 8 pulses to establish the accurate output regardless of the value of the analog input.
- However, one additional clock pulse is used to load the output register and reinitialize the circuit.
- The AD7592 (Analog Devices Co.), a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

Charge Balancing ADC

- The figure showing this type of conversion is shown below.

Charge Balancing ADC cntd..

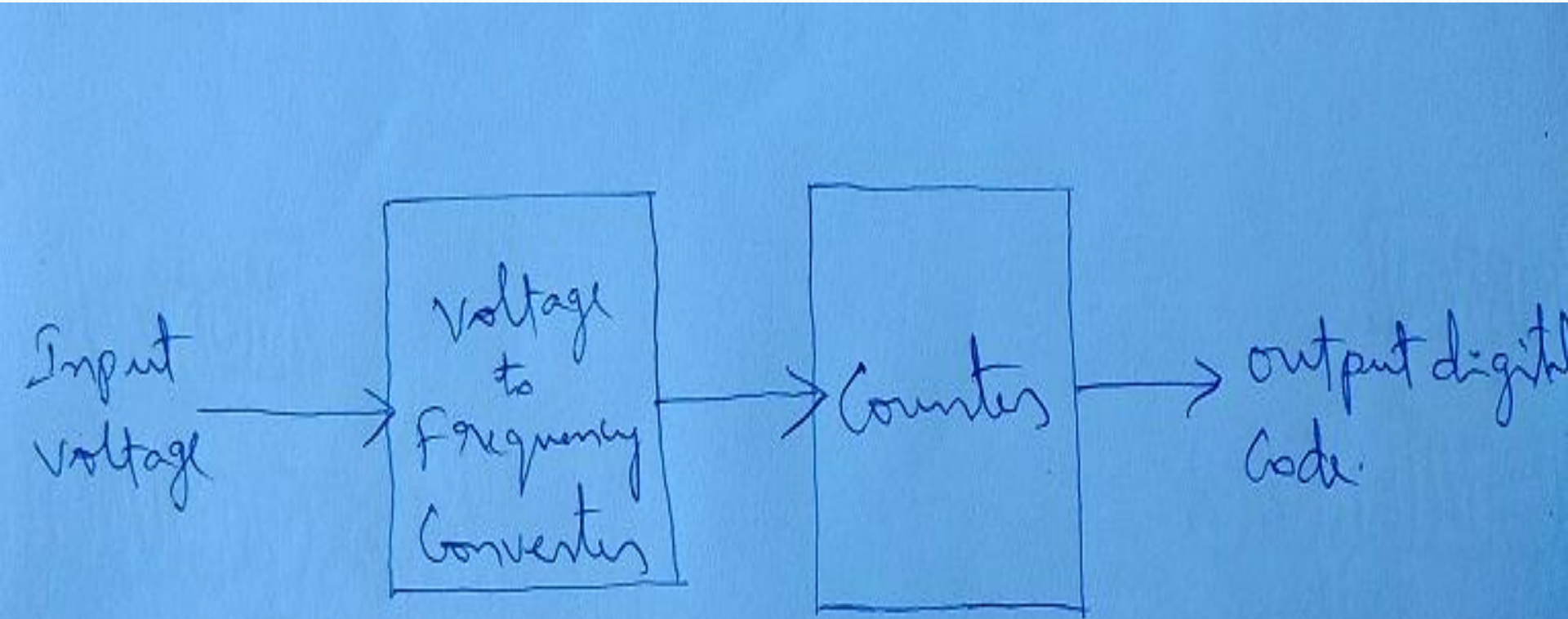


Fig Charge Balancing ADC

Charge Balancing ADC cntd..

- The principal of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency converter.
- This frequency is then measured by a counter and converted to an output code proportional to the analog input.
- The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form.
- However the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time.
- The drawback of the charge balancing ADC is eliminated by the Dual slope conversion.

DAC/ADC Specifications

- Both D/A and A/D converters are available with wide range of specifications.
- The various important specifications of converters generally specified by the manufacturers are analyzed
- The specifications are Resolution, Linearity, Accuracy, Monotonicity, settling time and stability.

Resolution:

- The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter.

DAC/ADC Specifications cntd..

- For example, an 8-bit D/A converter has 2^8 -1 =255 equal intervals. Hence the smallest change in output voltage is 1/255 of the full scale output range. In short, the resolution is the value of the LSB.

  Resolution (in volts) = Vfs/(2^n – 1)

Linearity:

- The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics.
- In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear.

DAC/ADC Specifications cntd..

Accuracy:

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
- Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Monotonicity:

- A monotonic DAC is the one whose analog output increases for an increase in digital input.
- A monotonic characteristic is essential in control applications, otherwise oscillations can result.

DAC/ADC Specifications cntd..

Settling time:

- The most important dynamic parameter is the settling time.
- It represents the time it takes for the output to settle with in a specified band + or – ½ LSB of its final value following a code change at the input (usually a full scale change).
- Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

DAC/ADC Specifications cntd..

Stability:

- The performance of converter changes with temperature, age and power supply variations.
- So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

End of Unit III

Unit IV

Digital Integrated Circuits

Classifications of Integrated Circuits

- The classifications of ICs are done as below.
  - Linear ICs
  - Digital ICs
- Based on the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.
- In Monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon.
- In Hybrid circuits, separate components parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds.

Classifications of Integrated Circuits cntd..

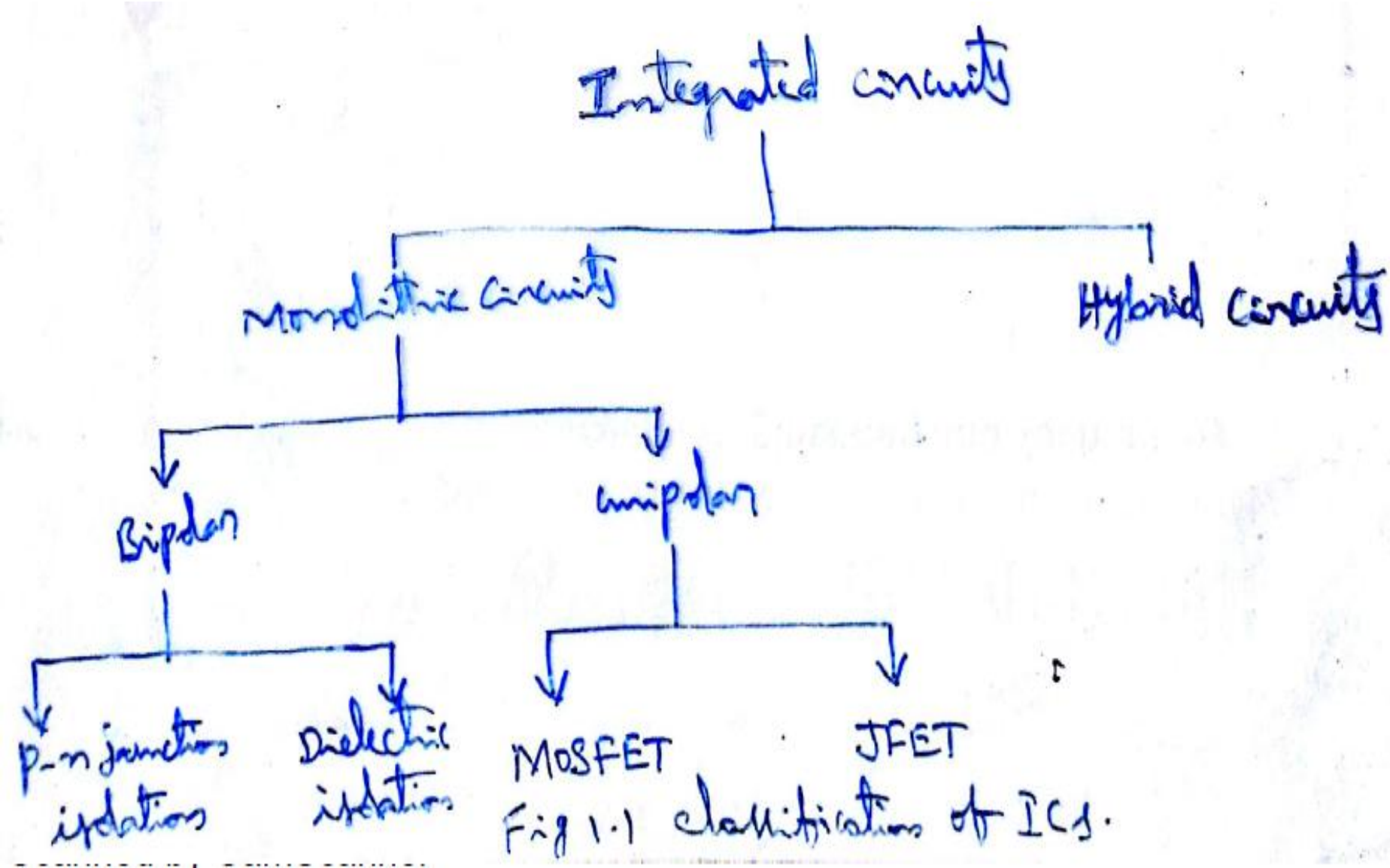


Fig 1.1 classification of ICs.

Parallel Binary Adders

Half Adder Logic:

- Binary addition is given by

  0 + 0 = 0

  0 + 1 = 1

  1 + 0 = 1

  1 + 1 = 10

- From the above rules of Binary addition, we have the half adder logic as

Parallel Binary Adders cntd..

$$\Sigma = A \oplus B \quad \text{and} \quad C_{out} = AB$$

Parallel Binary Adders cntd..

- By using above two equations, the logic diagram for half adder is given in the figure 6.10.

Parallel Binary Adders cntd..

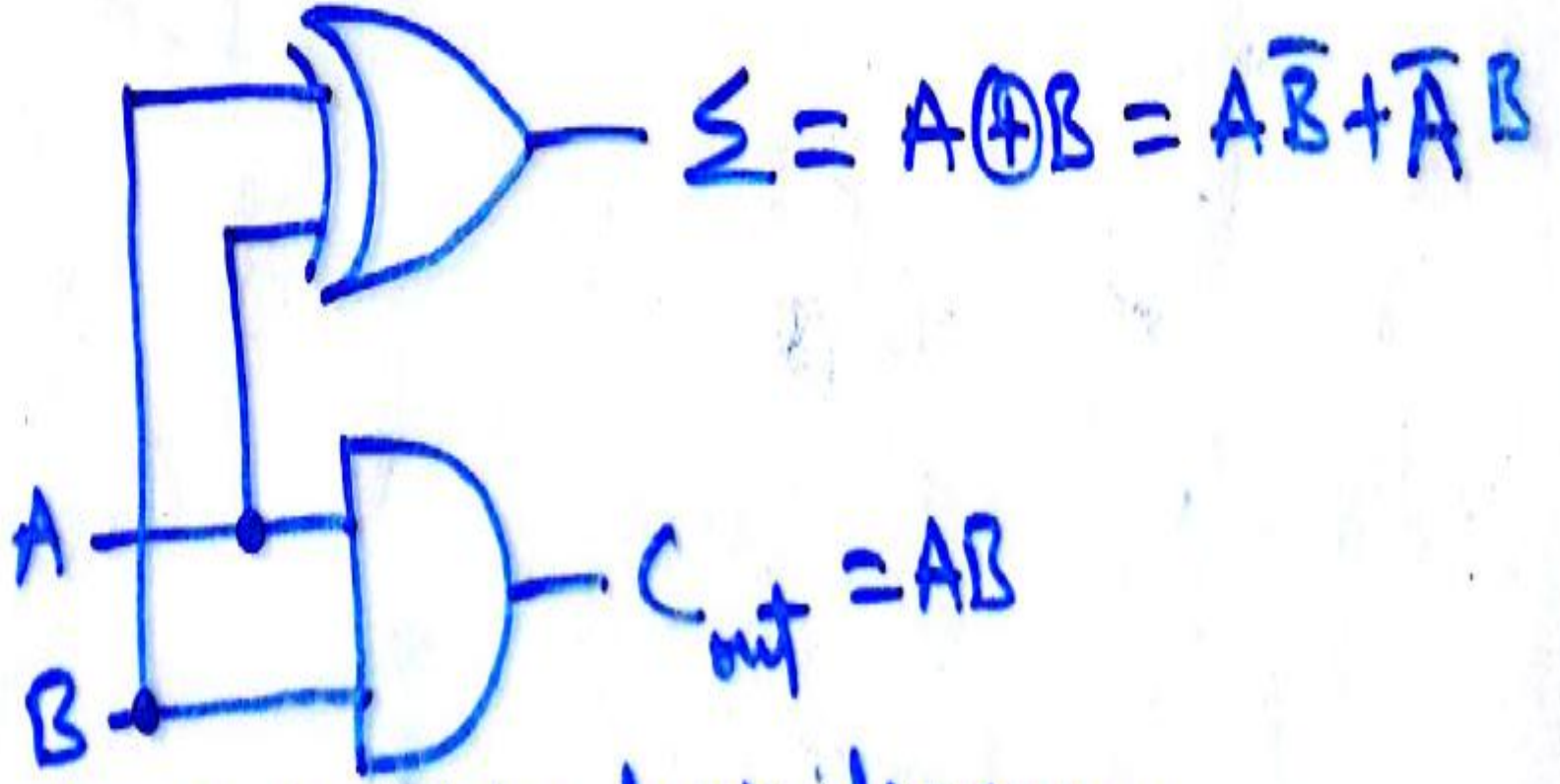


Fig 6-10 Half-adder logic diagram

Parallel Binary Adders cntd..

Full Adder Logic:

Truth Table

A	B	Cin	Cout	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Parallel Binary Adders cntd..

the logic is

$$\Sigma = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B) C_{in}$$

Parallel Binary Adders cntd..

- By using above two equations, we can have the logic diagram of full adder as shown in figure 6.12

Parallel Binary Adders cntd..

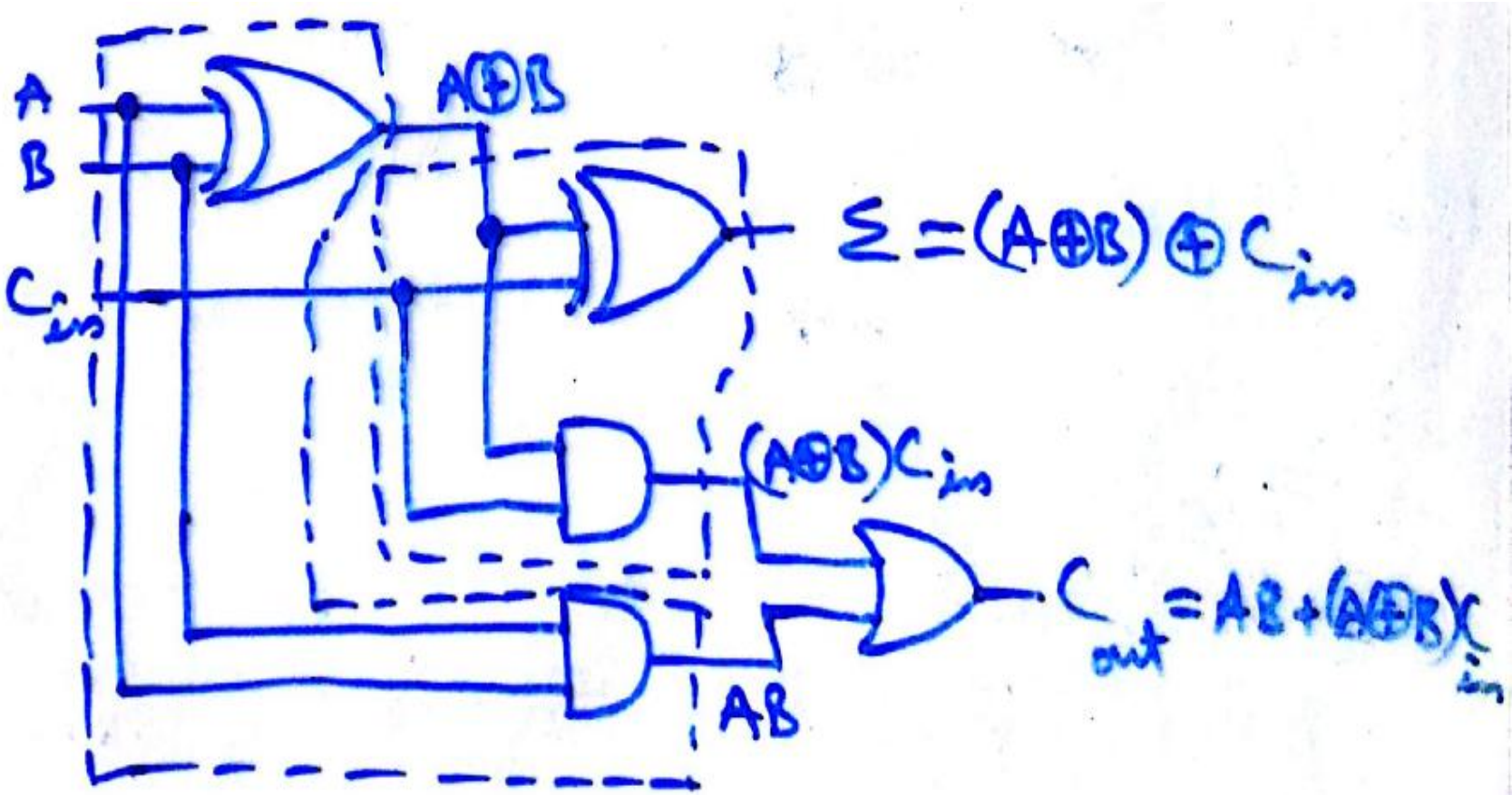
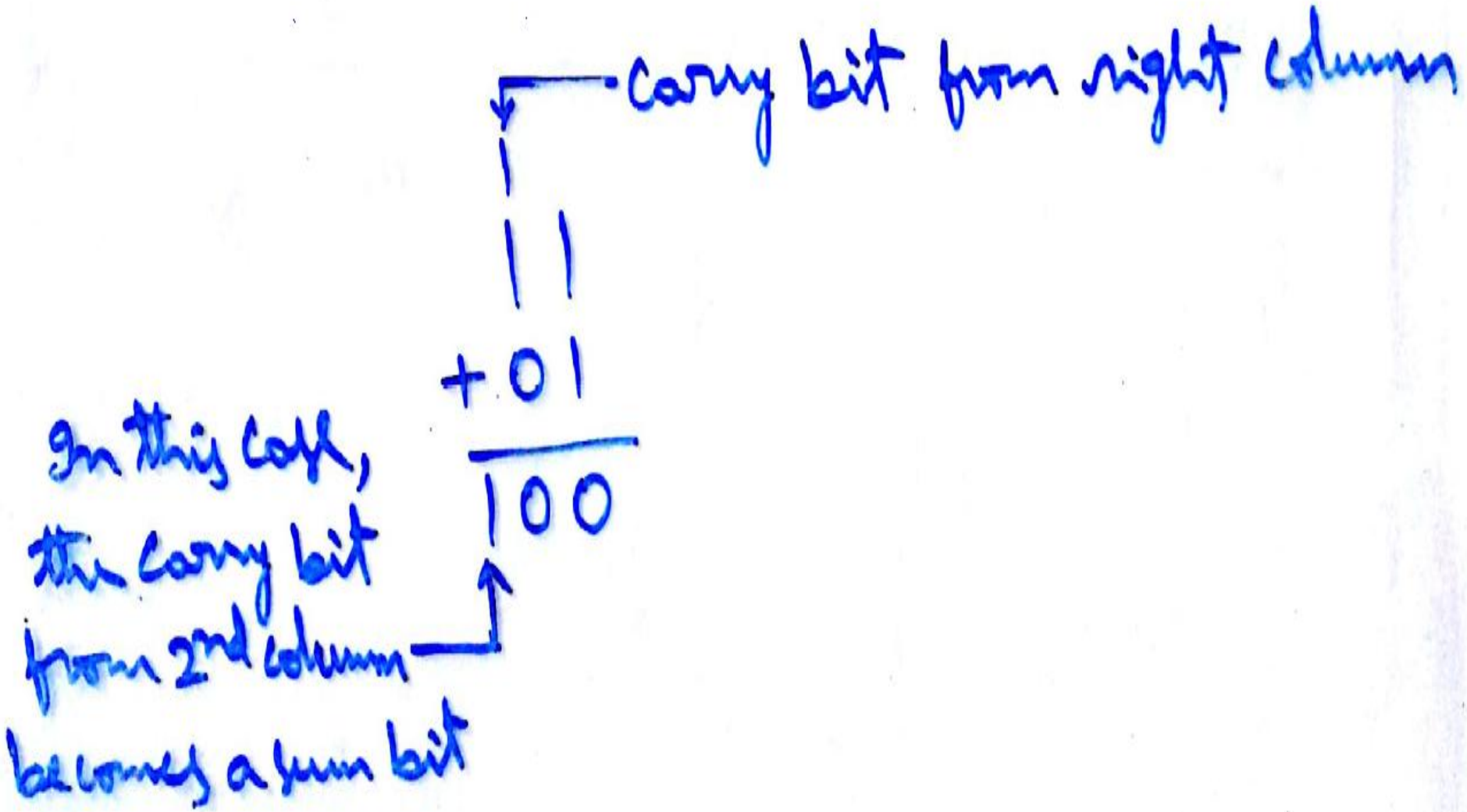


Fig 6-12 Fulladder logic diagram

Parallel Binary Adders cntd..

- The previous logic diagram can be replaced by two half adders.
- Parallel binary adder is obtained by connecting two or more full adders.
- Consider two 2-bit numbers addition which is given below.

Parallel Binary Adders cntd..



Parallel Binary Adders cntd..

- For each bit addition, one full adder is required, hence for 2 bit numbers addition we require 2 full adders.
- These two full adders are to be connected in parallel as shown in figure 6.15.

Parallel Binary Adders cntd..

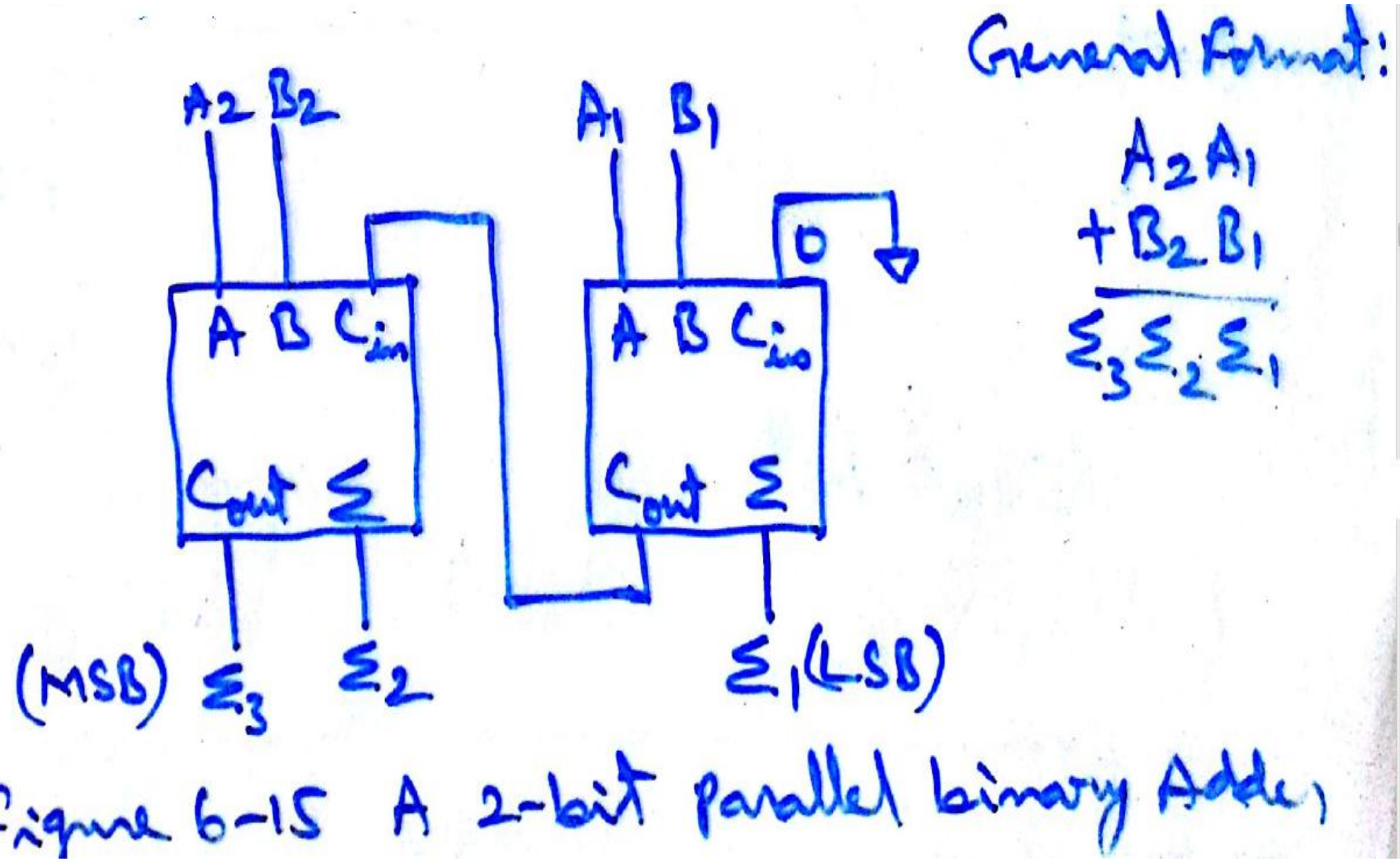


Figure 6-15 A 2-bit parallel binary Adder

Parallel Binary Adders cntd..

- Similarly a 4-bit parallel adder is given in Figure 6.17.

Parallel Binary Adders cntd..

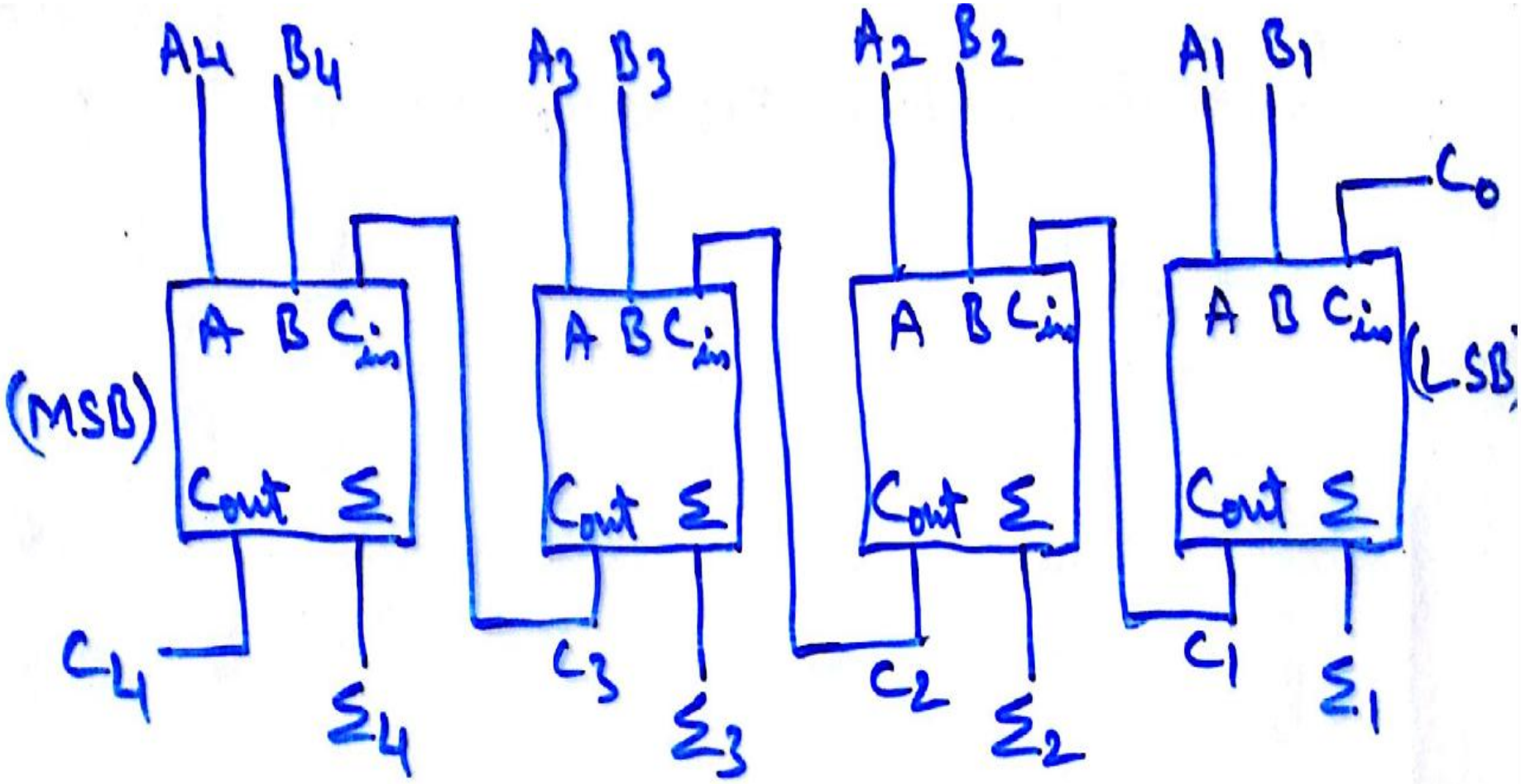
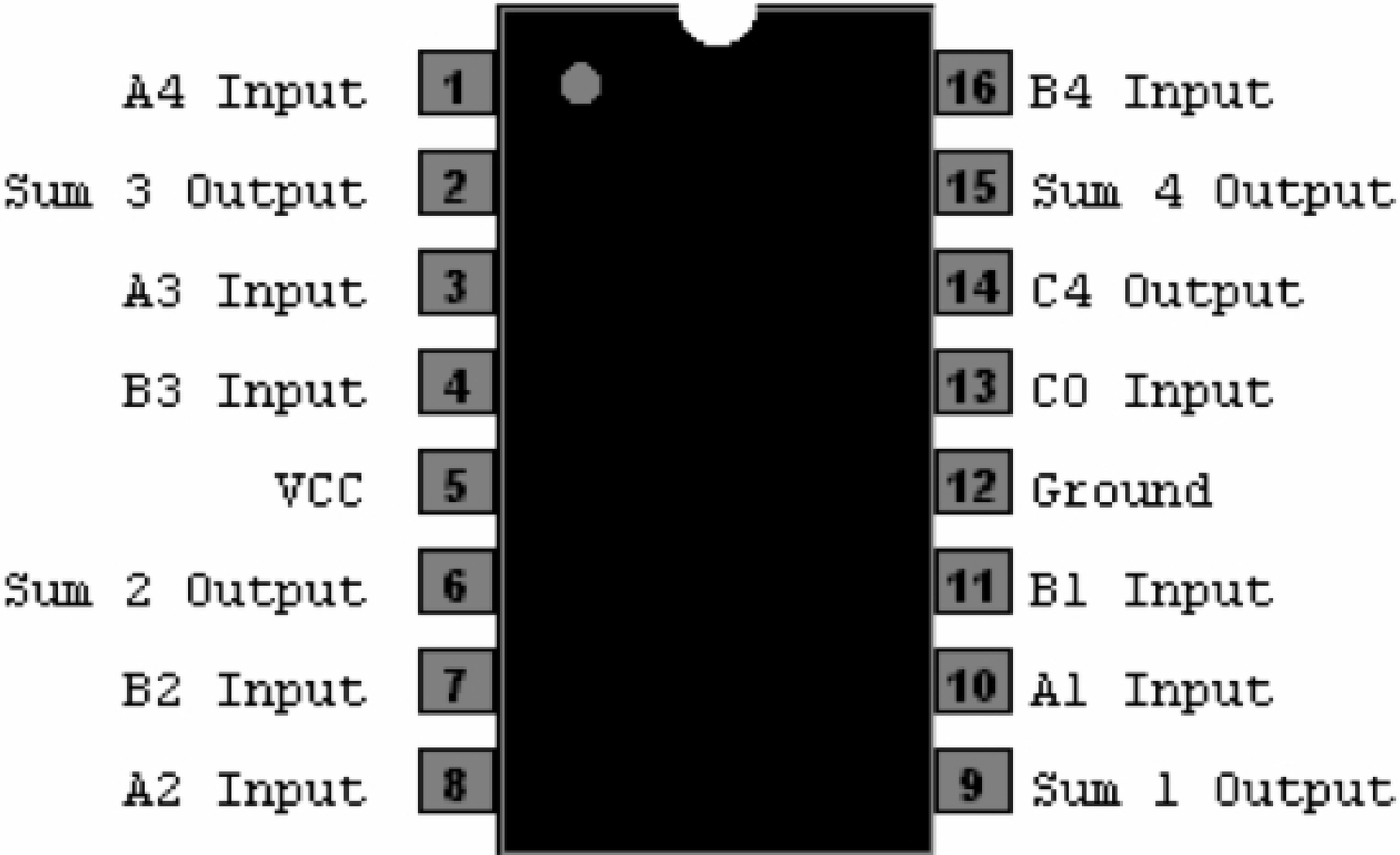


figure 6-17 A 4-bit parallel Adder.

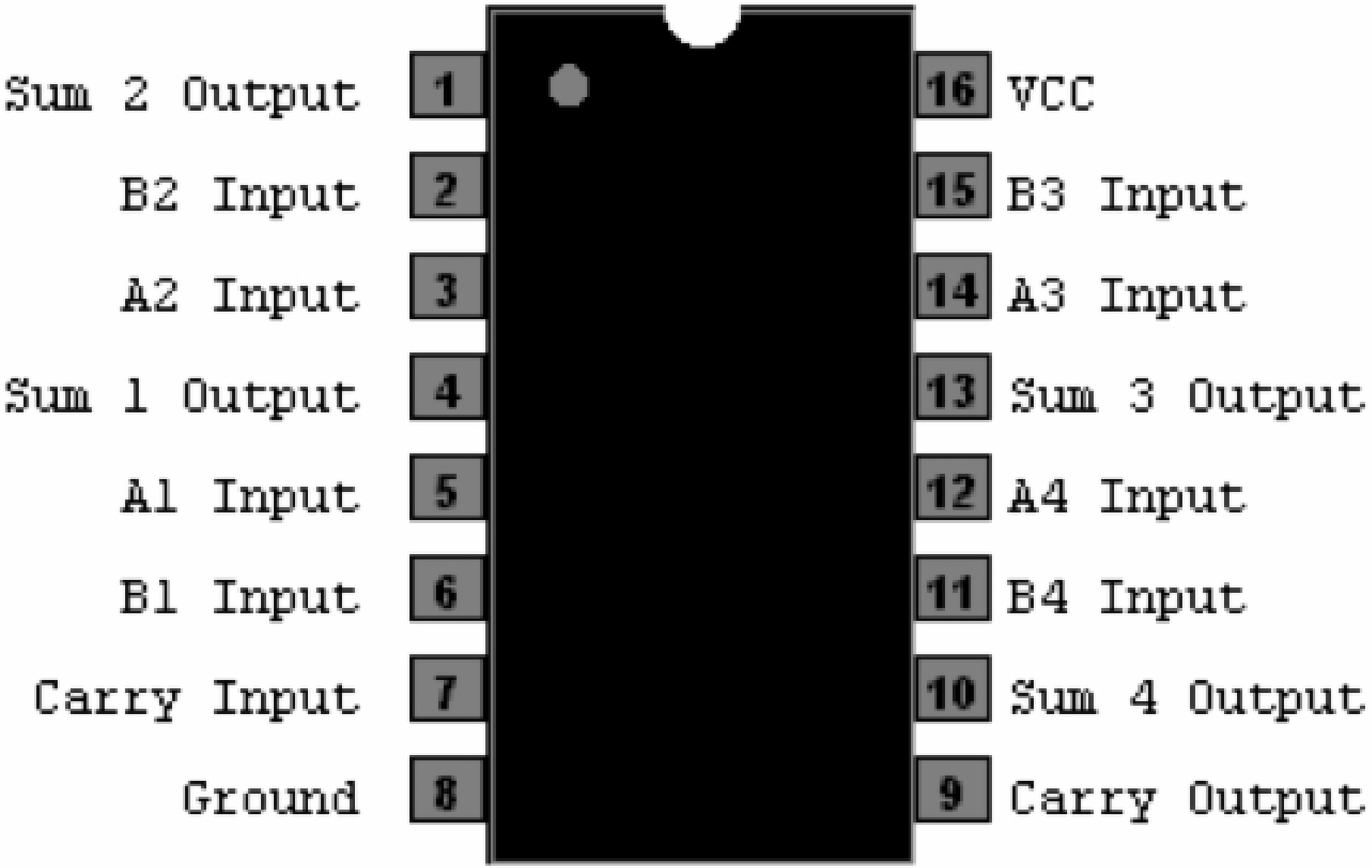
Parallel Binary Adders cntd..

- In the above diagram, C1, C2 and C3 are called carries and C0 is an external carry input and C4 is an output.
- Examples of 4-bit parallel adders that are available in IC form are the 74LS83A and the 74LS283 low-power Schottky TTL devices.
- These two ICs are functionally identical to each other but not pin compatible.
- Four 4-bit parallel adders are cascaded to form a 16-bit parallel adder.

Pin Diagram of 74LS83A



Pin Diagram of 74LS283



Parallel Binary Subtracter

- Subtraction is a special case of addition.
- For example, subtracting +6 (the subtrahend) from +9 (the minuend) is equivalent to adding -6 to +9.
- Basically, the subtraction operation changes the sign of the subtrahend and adds it to the minuend.
- The result of a subtraction is called the difference.

Comparators

- The exclusive OR gate can be used as a basic comparator because its output is a 1 if the two input lines/bits are not equal and a 0 if the input bits are equal.

Comparators cntd..

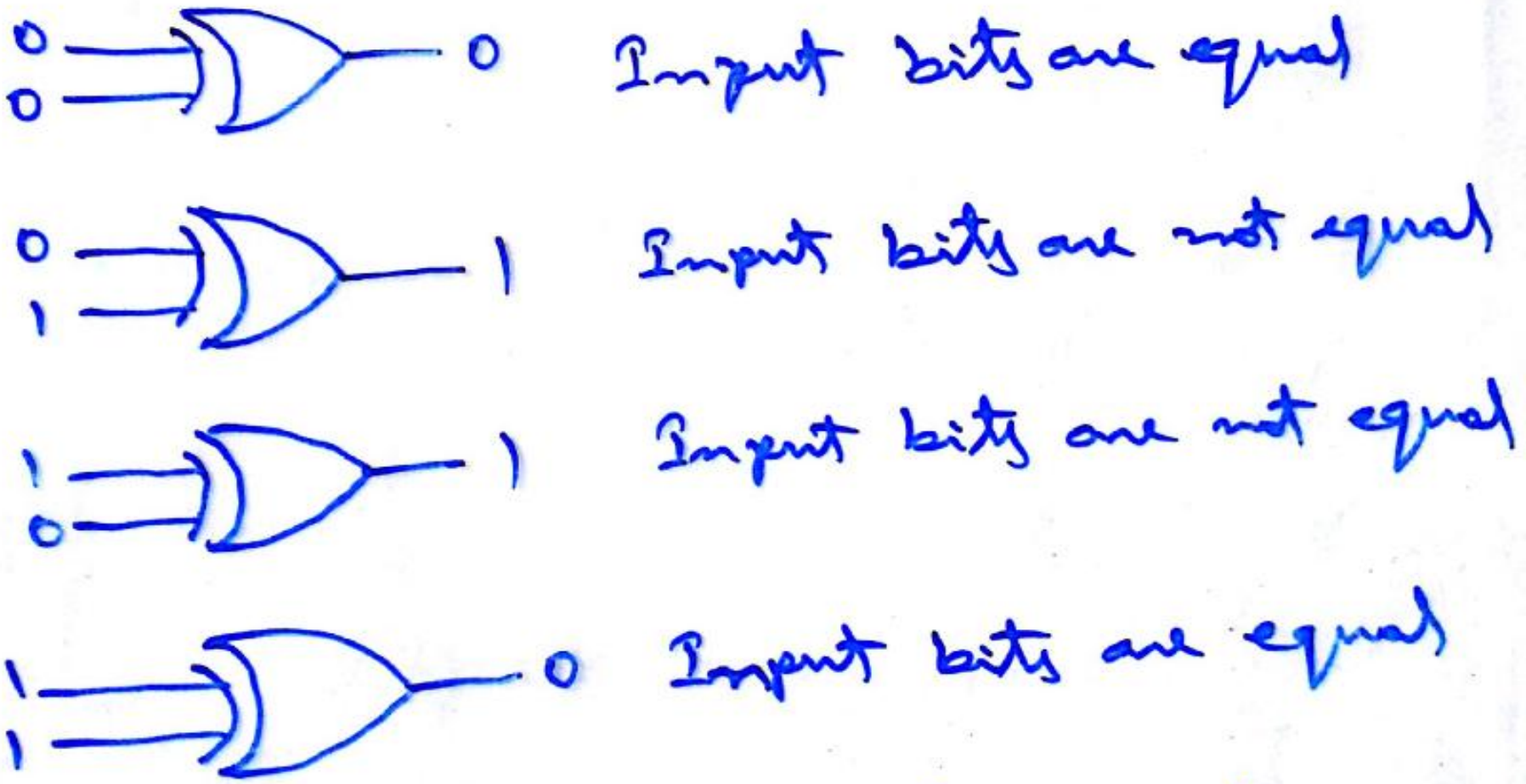


Figure 6-22 Basic Comparator operation

Comparators cntd..

- In order to compare 2- bit numbers, the diagram shown in Figure 6.24 is used.

Comparators cntd..

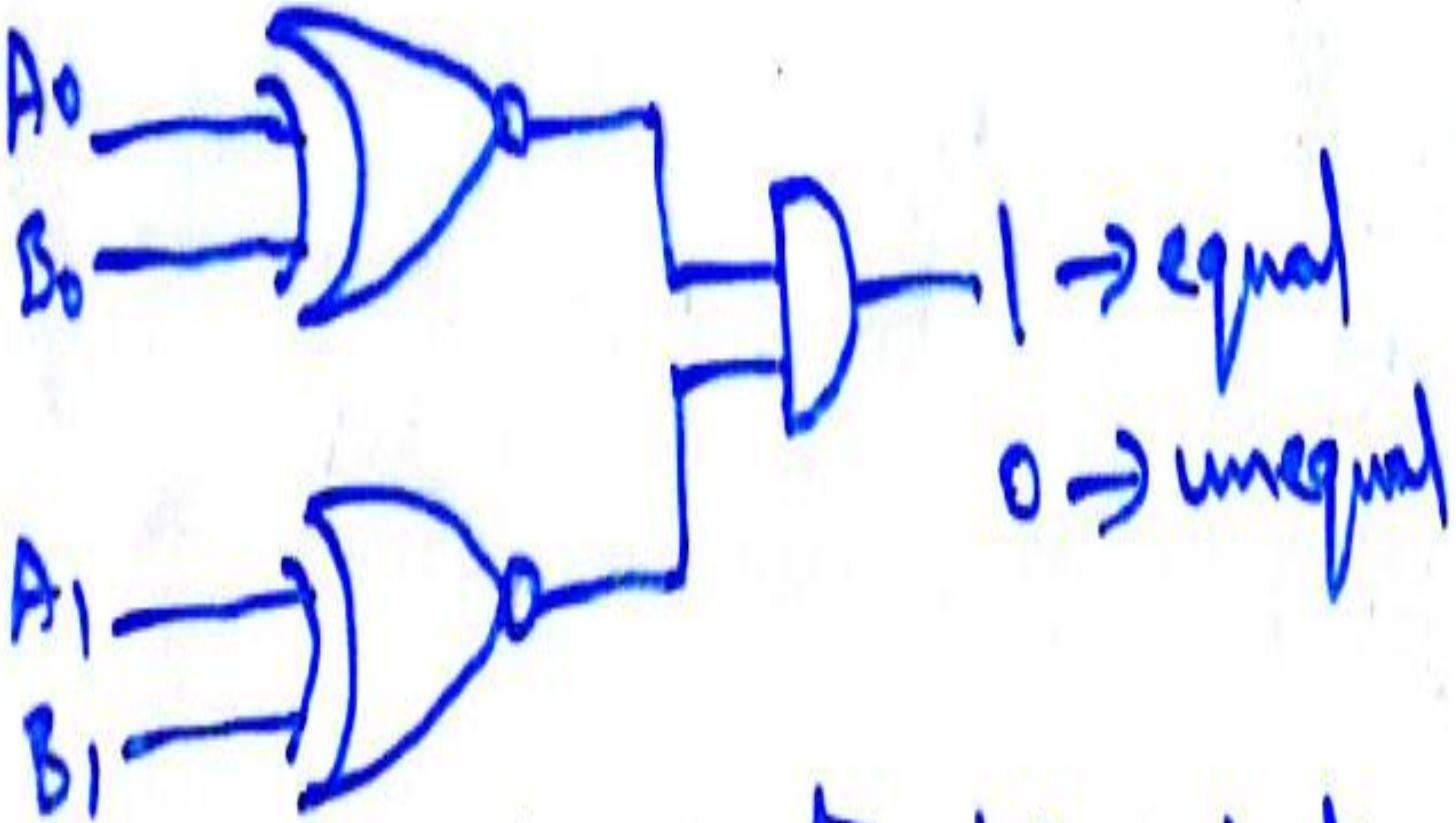


Figure 6-24 Comparator for 2-bit numbers

Comparators cntd..

- In addition to equality output, other outputs (A < B & A > B) are also provided by many IC Comparators.
- The diagram shown in Figure 6.25 is the logic symbol for a 4-bit comparator.

Comparators cntd..

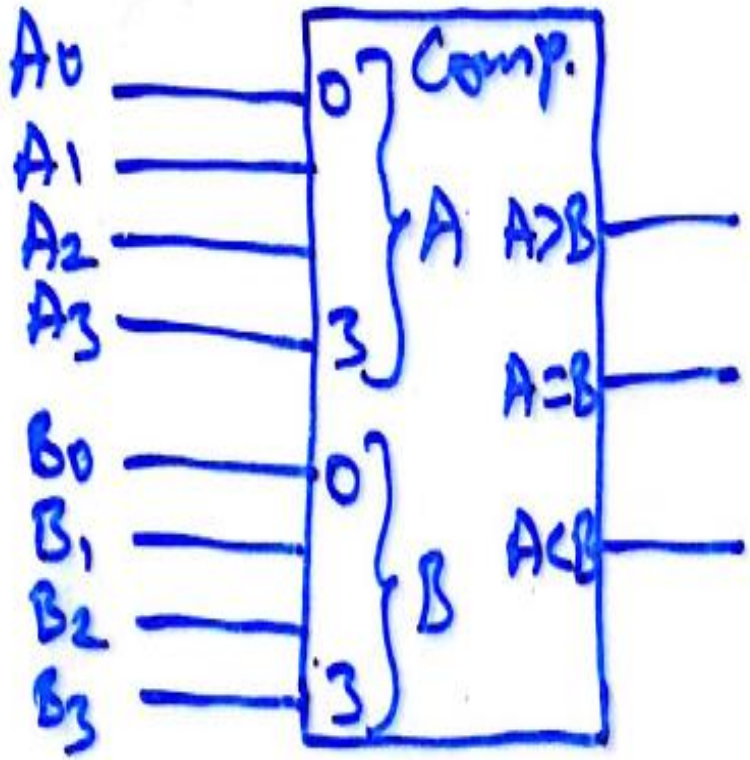


Figure 6-25 Logic symbol for a 4-bit comparator

Comparators cntd..

- To determine an inequality of binary numbers A and B, you first examine the highest order bit in each number.

1 If A3 =1 and B3=0, number A > number B

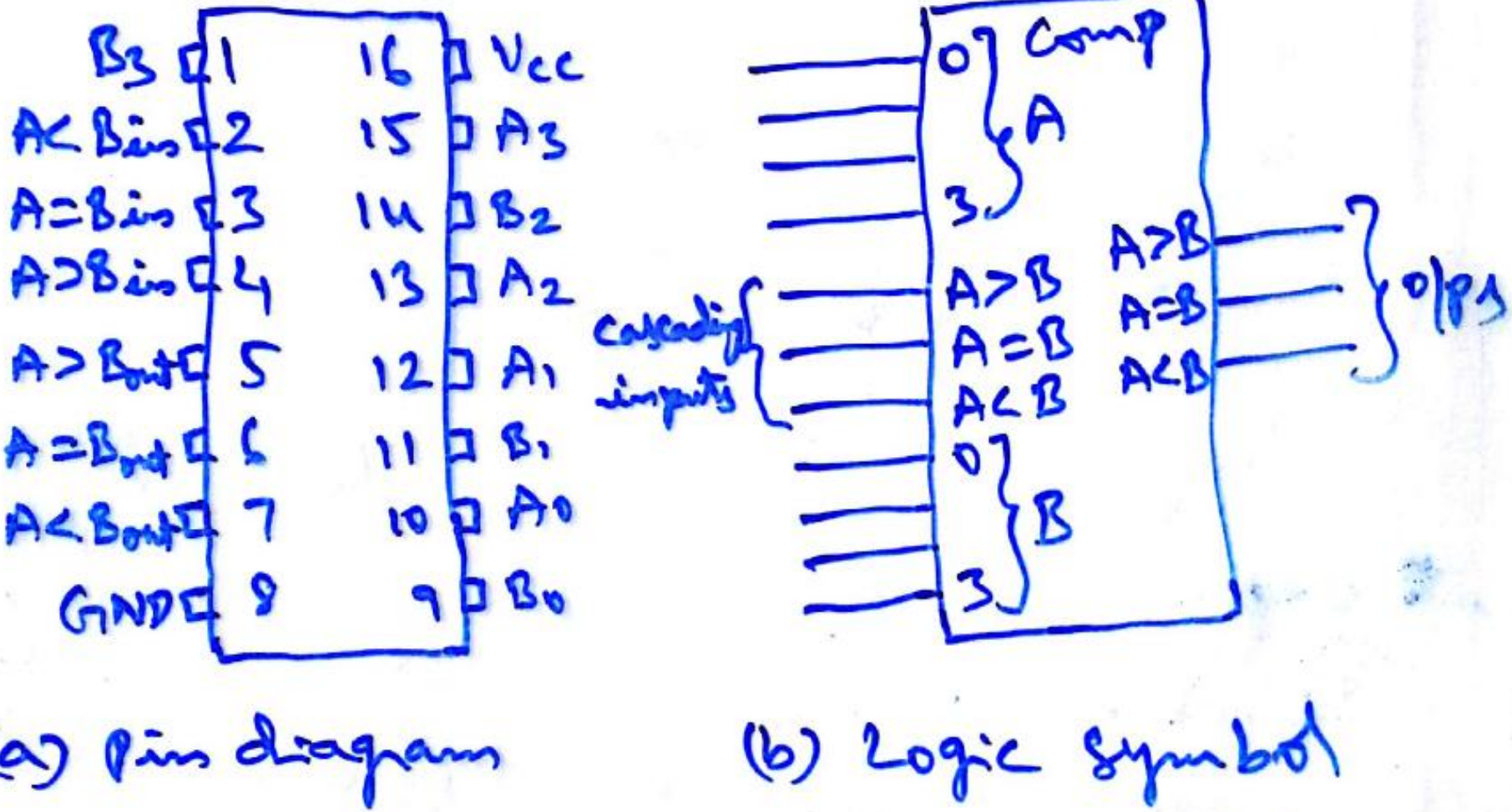
2 If A3 =0 and B3=1, number A < number B

3 If A3 = B3, then you must examine the next lower bit position.

A 4-Bit Magnitude Comparator

- The 74HC85 is a comparator whose pin diagram and logic symbol are shown in Figure 6.27.

A 4-Bit Magnitude Comparator cntd..



(a) Pin diagram

(b) Logic symbol

A 4-Bit Magnitude Comparator cntd..

- The above device has got 3 cascading inputs, A < B, A = B, A > B. These inputs allow several comparators to be cascaded for comparison of any number of bits greater than four.
- To expand the comparator, the A < B, A = B and A > B outputs of the lower order comparator are connected to the corresponding cascading inputs of the next higher-order comparator.
- The lowest order comparator must have a HIGH on the A = B input and LOWs on the A < B and A > B inputs.

A 4-Bit Magnitude Comparator cntd..

Example 1:

Use 74HC85 comparators to compare the magnitudes of 2 8-bit numbers. Show the comparators with proper interconnections.

Solution:

Two 74HC85s are required to compare two 8-bit numbers. They are connected as shown in the figure 6.28, in a cascaded arrangement.

A 4-Bit Magnitude Comparator cntd..

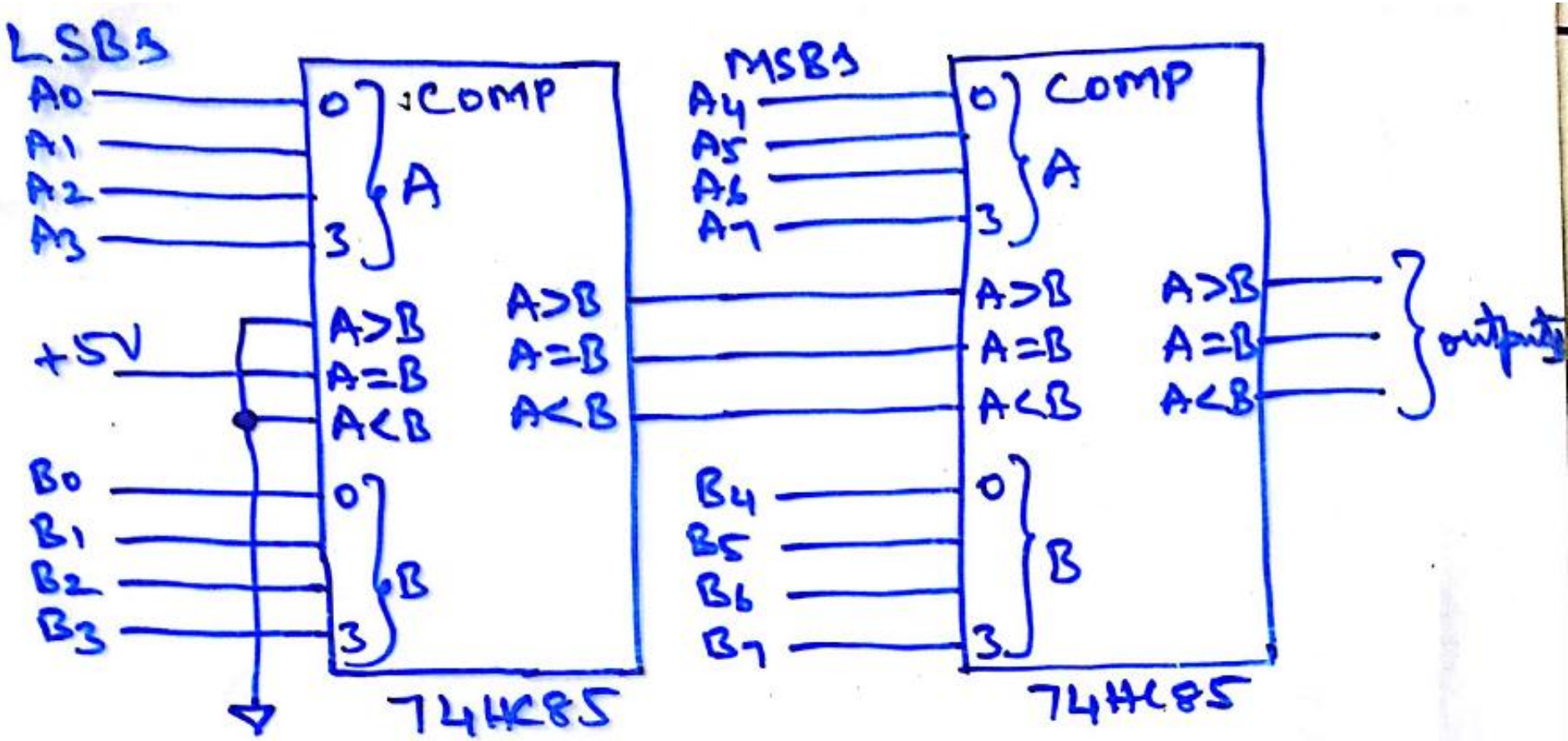


Figure 6-28 An 8-bit magnitude comparator using two 74HC85s.

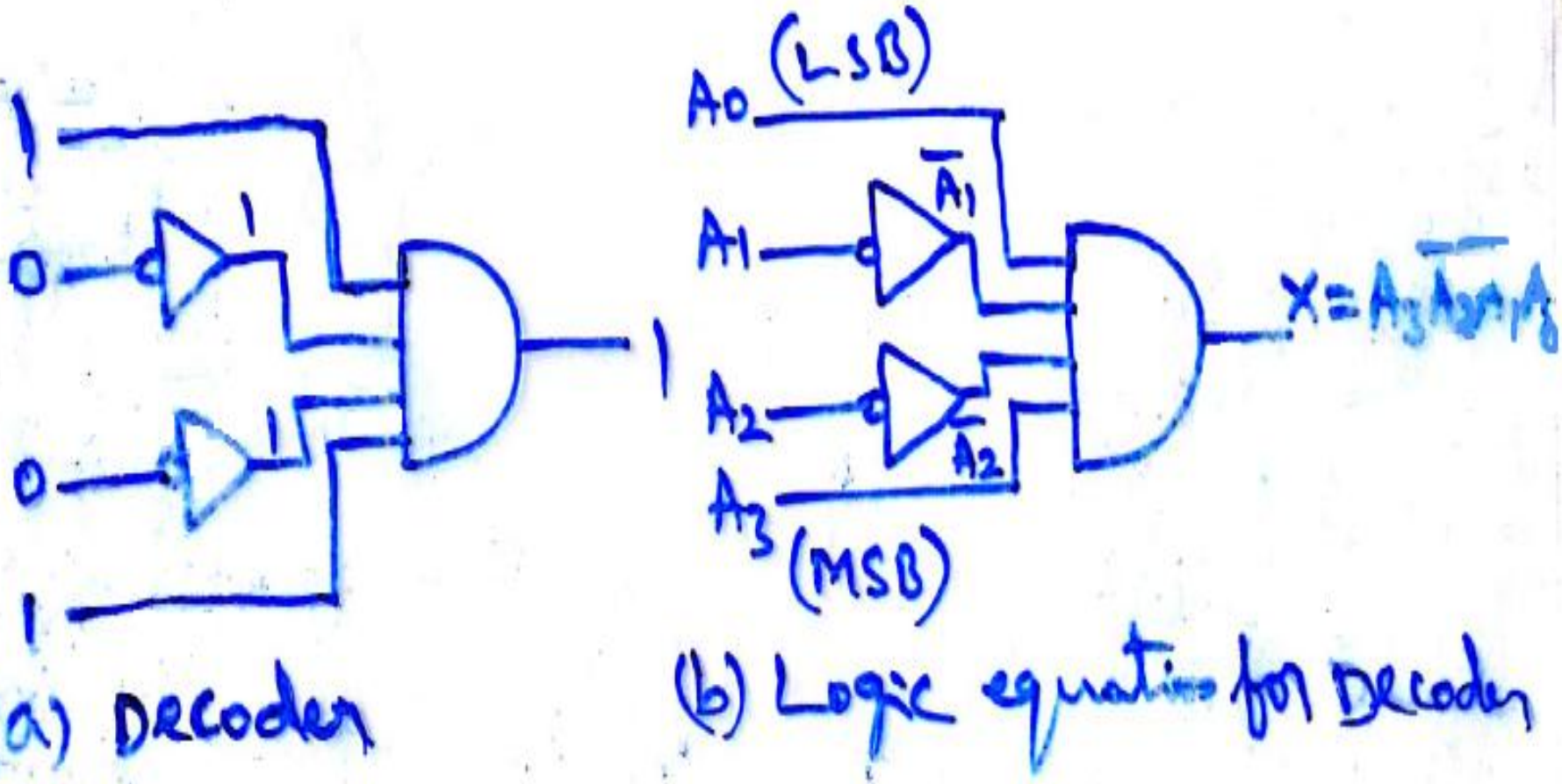
Decoders

- The basic function of a decoder is to detect the presence of a specified combination of bits (code) on its inputs and to indicate the presence of that code by a specified output level.
- In its general form, a decoder has n input lines to handle n bits and from one to 2^n output lines to indicate the presence of one or more n-bit combinations.

The Basic Binary Decoder

- Suppose, you need to determine when a binary 1001 occurs on the inputs of a digital circuit.
- An AND gate can be used as the basic decoding element because it produces a HIGH output only when all of its inputs are HIGH.
- Therefore, you must make sure that all of the inputs to the AND gate are HIGH when the Binary number 1001 occurs; this can be done by inverting the two middle bits (the 0s), as shown in the Figure 6.29

The Basic Binary Decoder cntd..



(a) Decoder (b) Logic equations for Decoder

Figure 6-29 Decoder and it's logic equations

The Basic Binary Decoder cntd..

- The logic equation for the decoder of Figure 6.29(a) is developed as illustrated in Figure 6.29(b)
- You should verify that the output is 0 except when A0=1, A1=0, A2=0, and A3=1 are applied to the input.
- If a NAND gate is used in place of the AND gate in Figure 6.29, a low output will indicate the presence of the proper binary code, which is 1001 in this case.

4-Bit Decoder

- In order to decode all possible combinations of four bits, sixteen decoding gates are required (2^4 = 16)
- This type of decoder is commonly called either a 4-line-to-16-line decoder because there are four inputs and sixteen outputs or a 1-of-16-decoder because for any given code on the inputs, one of the sixteen outputs is activated.
- A list of sixteen binary codes and their corresponding decoding functions is given in Table 6.4

4-Bit Decoder cntd..

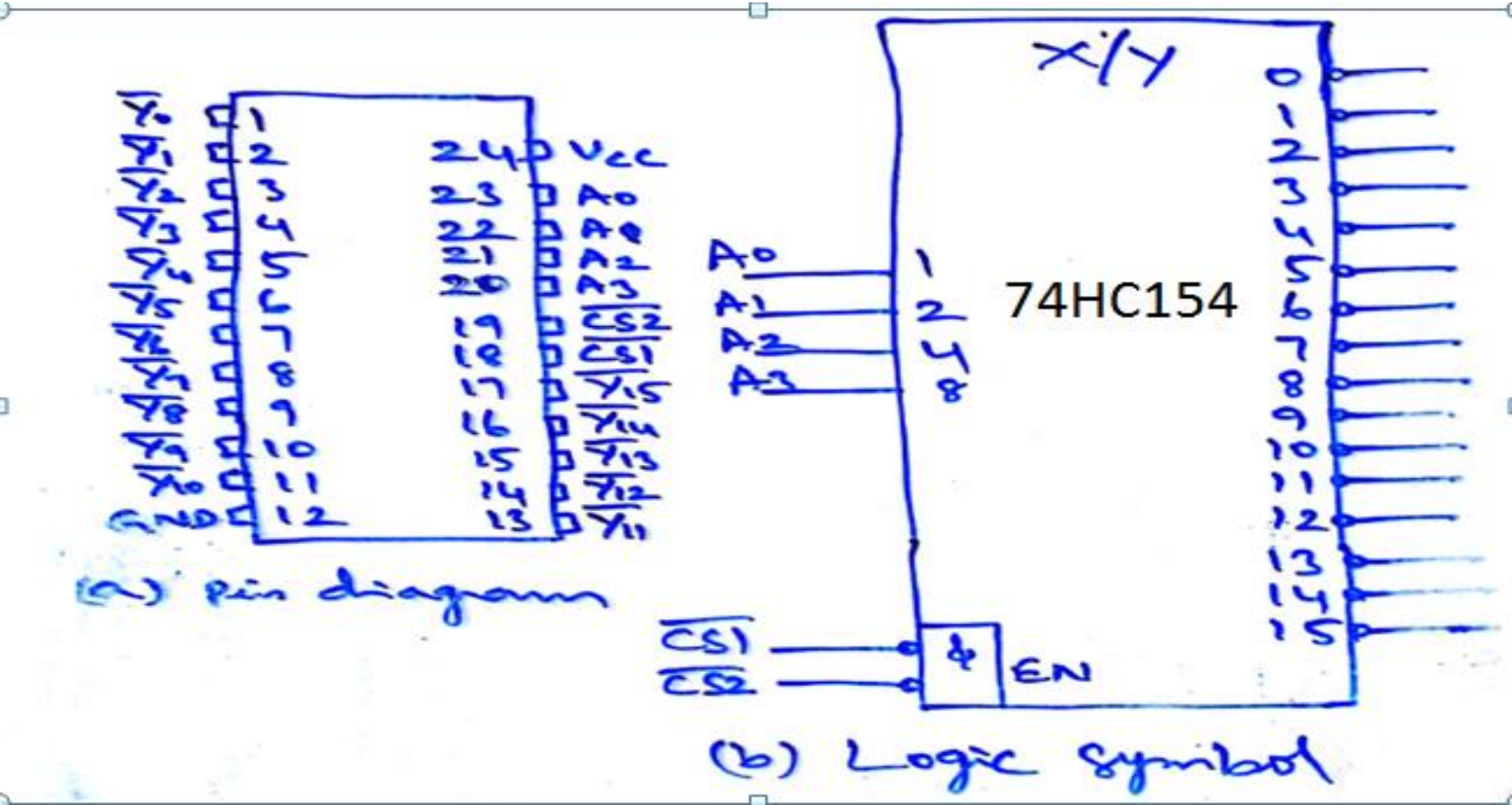
Decimal Digit	Bin. inputs A_3 A_2 A_1 A_0	Decoding Function	outputs 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0 0 0 0	$\bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0 0 0 1	$\bar{A}_3\bar{A}_2\bar{A}_1A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0 0 1 0	$\bar{A}_3\bar{A}_2A_1\bar{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0 0 1 1	$\bar{A}_3\bar{A}_2A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0 1 0 0	$\bar{A}_3A_2\bar{A}_1\bar{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0 1 0 1	$\bar{A}_3A_2\bar{A}_1A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0 1 1 0	$\bar{A}_3A_2A_1\bar{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0 1 1 1	$\bar{A}_3A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1 0 0 0	$A_3\bar{A}_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1 0 0 1	$A_3\bar{A}_2\bar{A}_1A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1 0 1 0	$A_3\bar{A}_2A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1 0 1 1	$A_3\bar{A}_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1 1 0 0	$A_3A_2\bar{A}_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1 1 0 1	$A_3A_2\bar{A}_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1 1 1 0	$A_3A_2A_1\bar{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1 1 1 1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Table 6-4

4-Bit Decoder cntd..

- If an active low output is required for each decoded number, the entire decoder can be implemented with NAND gates and inverters
- In order to decode each of the sixteen binary codes, sixteen NAND gates are required (AND gates can be used to produce active-HIGH outputs)
- The 74HC154 is good example of an IC decoder. The logic symbol is shown in Figure 6.32.

4-Bit Decoder cntd..



4-Bit Decoder cntd..

- There is an enable function (EN) provided on this device, which is implemented with a NOR gate used as a negative AND.
- A low level on each chip select input, $\overline{CS1}$ and $\overline{CS2}$, is required in order to make the enable gate output(EN) HIGH.
- The enable gate output is connected to an input of each NAND gate in the decoder, so it must be HIGH for the NAND gates to be enabled.
- If the enable gate is not activated by a LOW on both inputs, then all sixteen decoder outputs(Y) will be HIGH regardless of the states of the four input variables, A0, A1, A2 and A3.

The BCD-to-Decimal Decoder

- The BCD-to-Decimal decoder converts each BCD code (8421 code) into one of ten possible decimal digit indications. It is frequently referred as a 4-line-to-10-line decoder or a 1-of-10 decoder
- The method of implementation is the same as for the 1-of-16 decoder previously discussed, except that only ten decoding gates are required because the BCD code represents only the ten decimal digits 0 through 9.
- A list of the ten BCD codes and their corresponding decoding functions is given in table 6.5.

The BCD-to-Decimal Decoder cntd..

Decimal Digit	BCD code A_3	A_2	A_1	A_0	Decoding Function
0	0	0	0	0	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$
1	0	0	0	1	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,A_0$
2	0	0	1	0	$\overline{A_3}\,\overline{A_2}\,A_1\,\overline{A_0}$
3	0	0	1	1	$\overline{A_3}\,\overline{A_2}\,A_1\,A_0$
4	0	1	0	0	$\overline{A_3}\,A_2\,\overline{A_1}\,\overline{A_0}$
5	0	1	0	1	$\overline{A_3}\,A_2\,\overline{A_1}\,A_0$
6	0	1	1	0	$\overline{A_3}\,A_2\,A_1\,\overline{A_0}$
7	0	1	1	1	$\overline{A_3}\,A_2\,A_1\,A_0$
8	1	0	0	0	$A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$
9	1	0	0	1	$A_3\,\overline{A_2}\,\overline{A_1}\,A_0$

Table 6-5.

The BCD-to-Decimal Decoder cntd..

- Each of these decoding functions is implemented with NAND gates to provide active-low outputs
- If an active HIGH output is required, AND gates are used for decoding.
- The logic is identical to that of the first ten decoding gates in the 1-of-16 decoder.

Encoders

- An encoder is a combinational logic circuit that essentially performs a “reverse” decoder function.
- An encoder accepts an active level on one of its inputs representing a digit, such as a decimal or octal digit, and converts it to a coded output such as BCD or binary.
- Encoders can also be devised to encode various symbols and alphabetic characters.
- The process of converting from familiar symbols or numbers to a coded format is called encoding.

Encoders cntd..

- This type of encoder has ten inputs – one for each decimal digit and four outputs corresponding to the BCD code, as shown in figure 6.37. this is a 10-line-to-4-line encoder.

Encoders cntd..

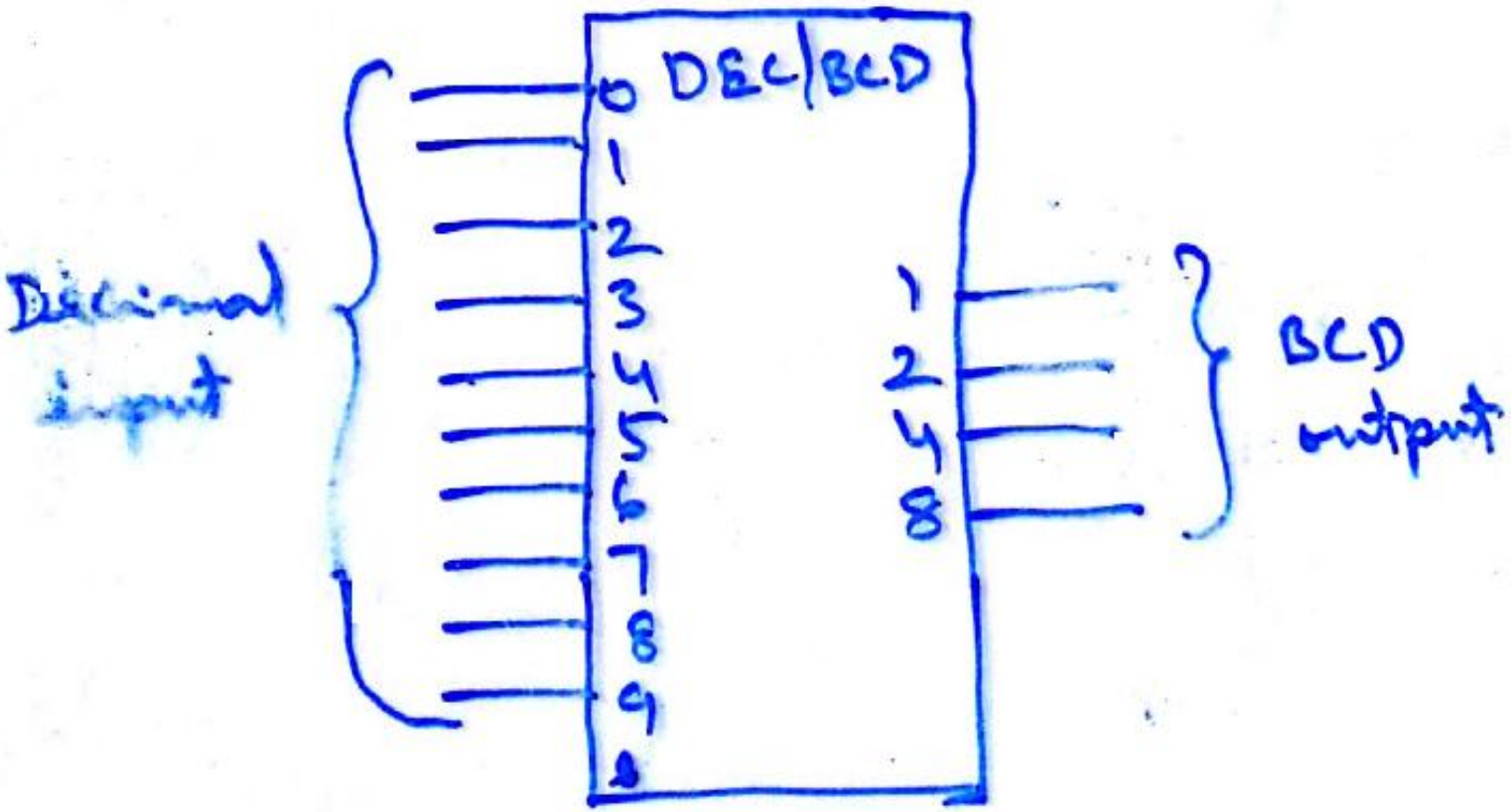


Figure 6-37 Logic symbol for a decimal-to-BCD encoder.

Encoders cntd..

- The BCD (8421) code is listed in table 6.6

Encoders cntd..

Decimal Digit	BCD Code A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Table 6-6

Encoders cntd..

- From this table you can determine the relationship between the BCD bit and the decimal digits in order to analyze the logic.
- For instance, the most significant bit of the BCD code, A3, is always a 1 for decimal digits 8 or 9. An OR expression for bit A3 in terms of the decimal digits can therefore be written as

  $A3 = 8 + 9$

- Bit A2 is always a 1 for decimal digit 4,5,6, or 7 and can be expressed as an OR function as follows $A2 = 4 + 5 + 6 + 7$

Encoders cntd..

- Bit A1 is always a 1 for decimal digit 2,3,6 or 7 and can be expressed as A1 = 2+3+6+7
- Finally, A0 is always a 1 for decimal digit 1,3,5,7, or 9. The expression for A0 is

$$A0 = 1 + 3 + 5 + 7 + 9$$

- From these expressions just developed, we can obtain the encoder logic required which is shown in figure 6.38.
- svgsidfvdfv

Encoders cntd..

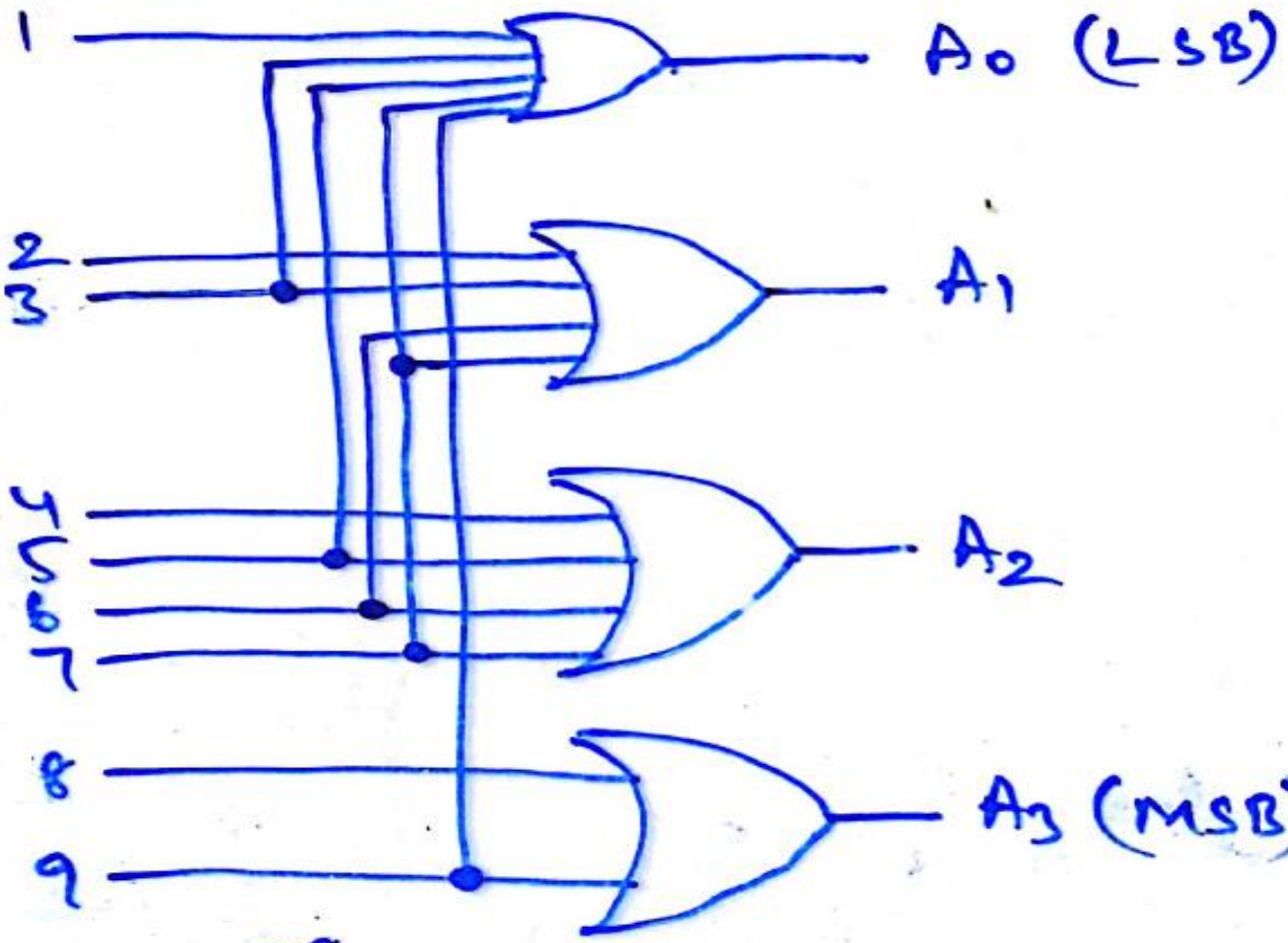


Figure : 6-38 : The encoder Logic diagram

Encoders cntd..

- The basic operation of the circuit in Figure 6.38 is as follows.
- When a high appears on one of the decimal digit input lines, the appropriate levels occur on the four BCD output lines.
- For instance, if input line 9 is HIGH (assuming all other input lines are LOW), this condition will produce a HIGH on outputs A0 and A3 and LOWs on outputs A1 and A2, which is the BCD code (1001) for decimal 9.

Encoders cntd..

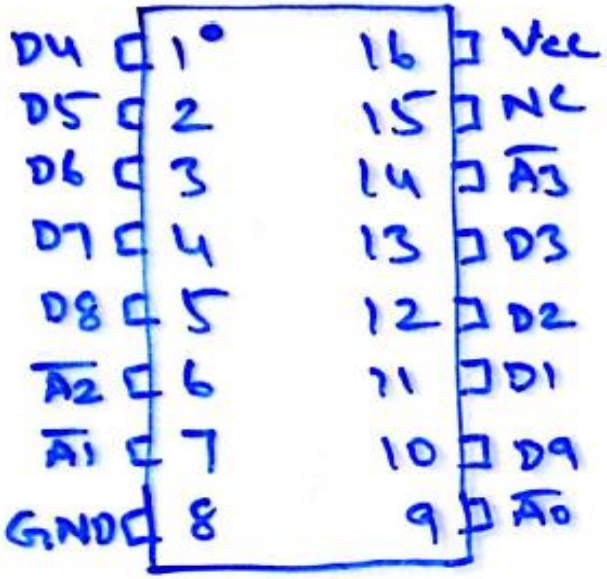
The Decimal-to-BCD Priority Encoder:

- This type of encoder performs the same basic encoding function as previously discussed.
- It also offers additional flexibility that it can be used in applications that require priority detection.
- The priority function means that the encoder will produce a BCD output corresponding to the highest order decimal digit input that is active and will ignore any other lower-order active inputs.

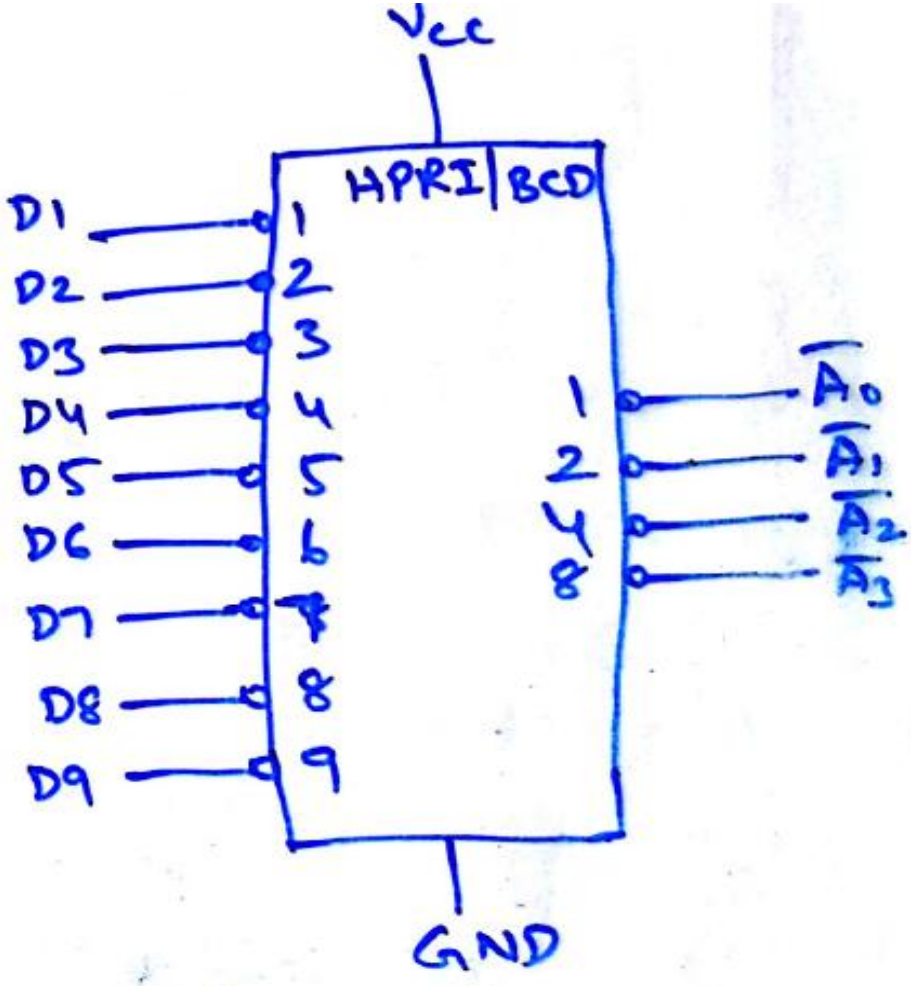
Encoders cntd..

- For instance, if the 6 and the 3 inputs are both active, the BCD output is 0110 (which represents decimal 6).
- The 74HC147 is a priority encoder with active LOW inputs (0) for decimal digits 1 through 9 and active LOW BCD outputs as indicated in the logic symbol in Figure 6.42.
- A BCD zero output is represented when none of the inputs is active.

Encoders cntd..



(a) pin diagram



(b) Logic diagram

Fig 6.42: For 74HC147

Encoders cntd..

- One classic application example for the above priority encoder is a keyboard encoder.

Code Converters

Binary-to-Gray and Gray-to-Binary conversion

The Gray Code:

- The gray code is unweighted and is not an arithmetic code; that is, there are no specific weights assigned to the bit positions.
- The important feature of the Gray code is that it exhibits only a single bit change from one code word to the next in sequence.
- This property is an important one in many applications, such as shaft position encoders, where error susceptibility increases with the number of bit changes between adjacent numbers in a sequence.

Code Converters cntd..

Example of Four-bit Gray code

Decimal	Binary	Gray code
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101

Code Converters cntd..

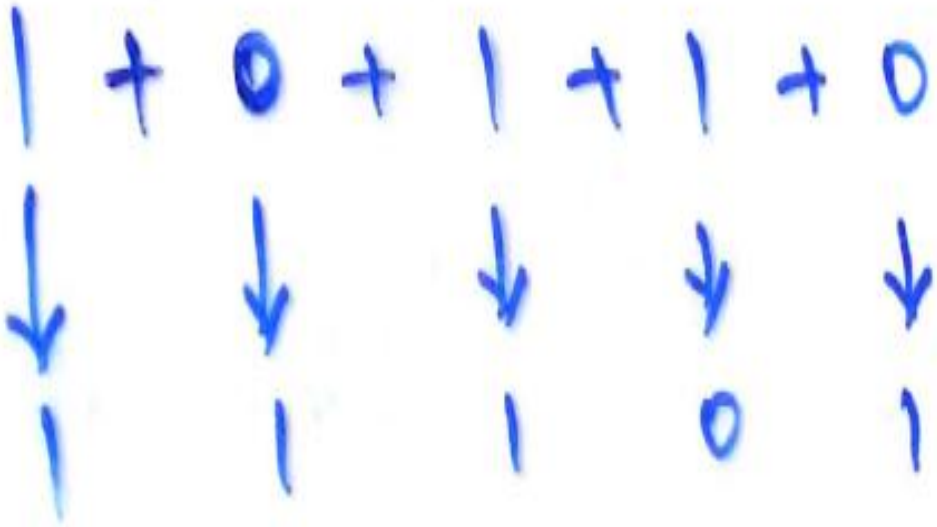
Binary to Gray Code Conversion

Rules:

1. The MSB in the Gray code is the same as the corresponding MSB in the Binary number
2. Going from left to right, add each adjacent pair of binary code bits to get the next Gray code bit. Discard carries.

Code Converters cntd..

Eg: Conversion of binary no. 10110 to Gray code



∴ the Gray code is 11101

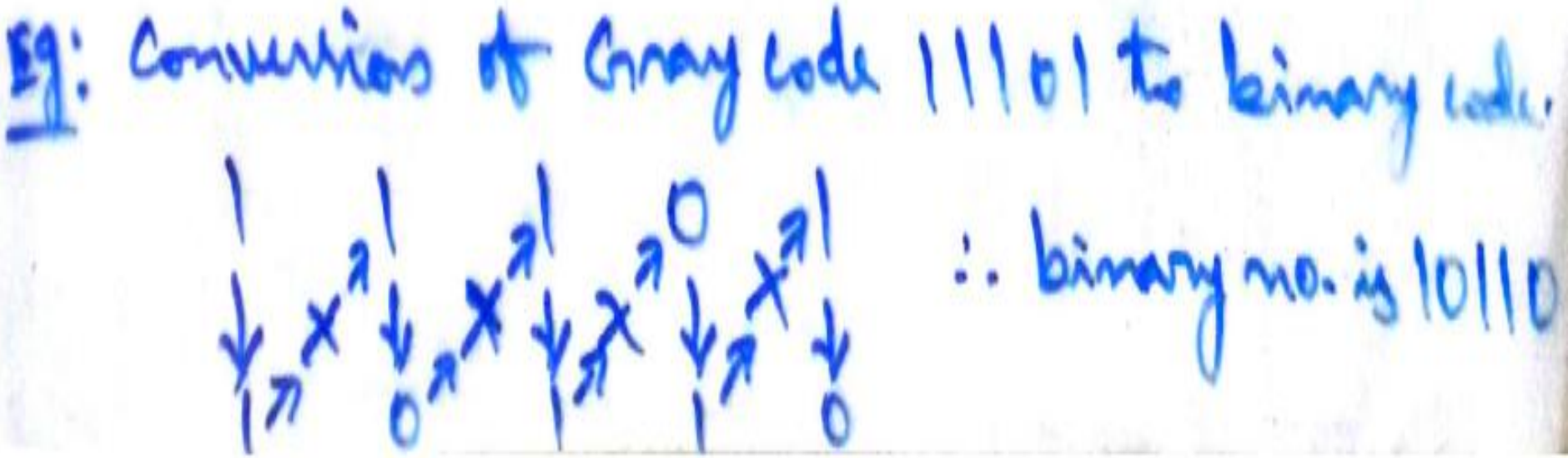
Code Converters cntd..

Gray to Binary Conversion

Rules

1. The MSB in the Binary code is the same as the corresponding bit in the Gray code
2. Add each Binary code bit generated to the Gray code bit in the next adjacent position. Discard carries.

Code Converters cntd..



Code Converters cntd..

- Exclusive-OR gates can be used for these conversions.
- Figure 6.46 shows a 4-bit Binary-to-Gray code converter and Figure 6.47 illustrates a 4-bit Gray-to-Binary converter.

Code Converters cntd..

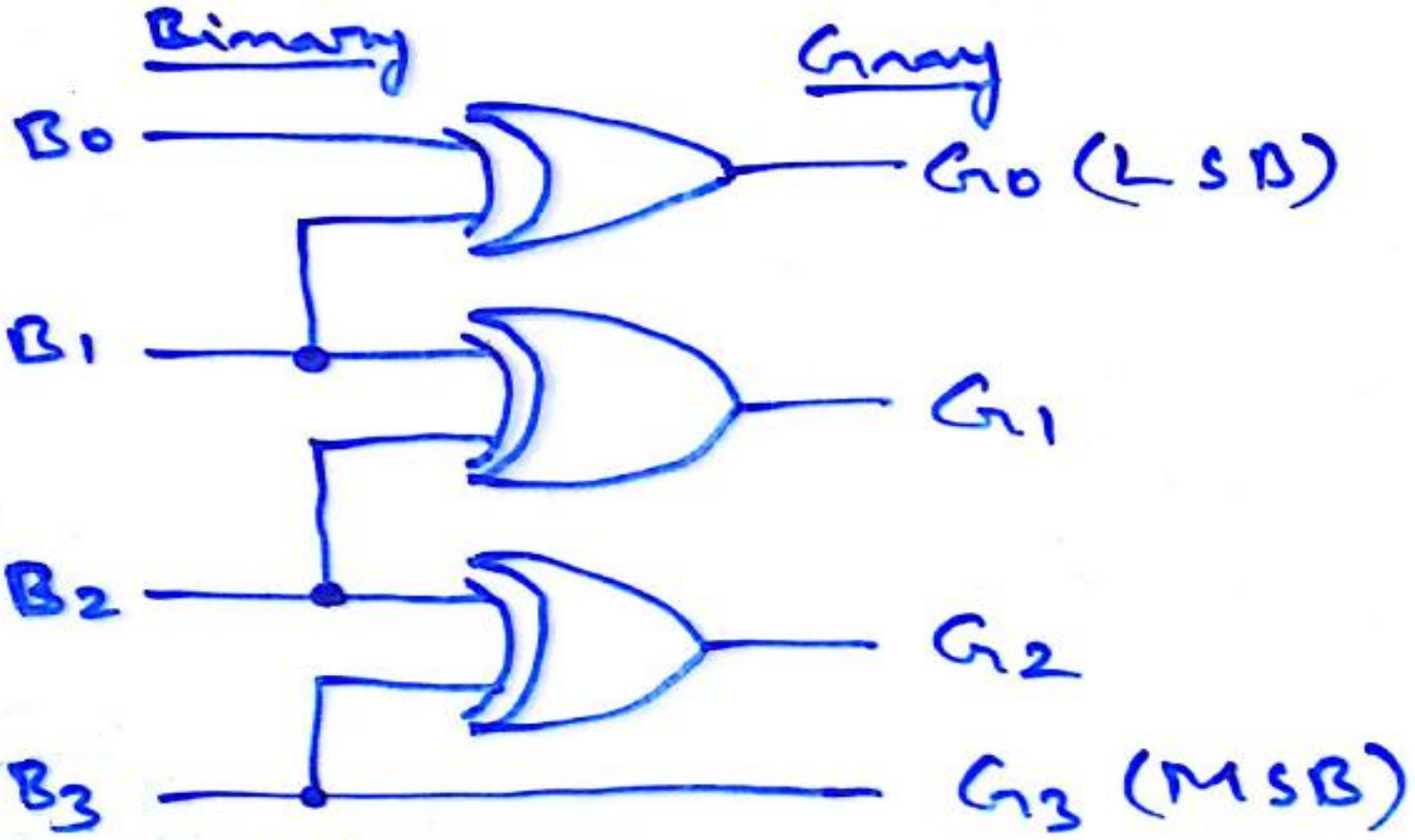


Figure 6-4b

Code Converters cntd..

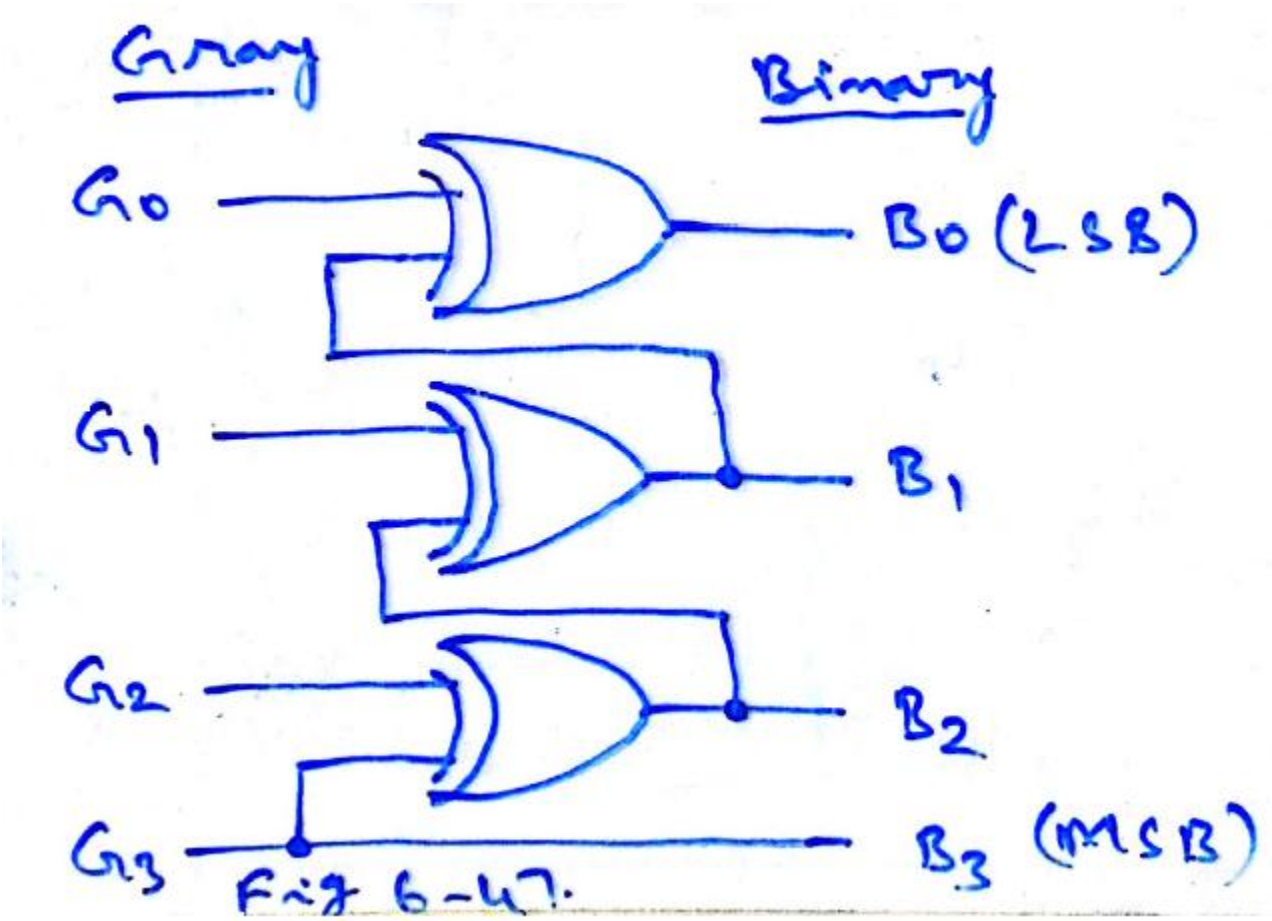


Fig 6-47.

Code Converters cntd..

BCD to Binary Conversion

- One method of BCD-to-Binary code conversion uses adder circuits. The basic conversion process is as follows.

1. The value, or weight, of each bit in the BCD number is represented by a Binary number.
2. All of the Binary representations of the weights of bits that are 1s in the BCD number are added.
3. The result of this addition is the Binary equivalent of the BCD number.

- A more concise statement of this operation is
  - The Binary numbers representing the weights of the BCD bits are summed to produce the total Binary number

Code Converters cntd..

- Let's take a decimal number 87. This can be written as 8 7

  1000 0111

  The left most 4-bit group represents 80 and the right most 4-bit group represents 7
- That is, the left most group has a weight of 10, and the right most group has weight of 1.
- Within each group, the binary weight of each bit is as follows.

Code Converters cntd..

	Tens Digit	Units Digit
Weight:	80 40 20 10	8 4 2 1
Bit designation:	B3 B2 B1 B0	A3 A2 A1 A0

- If the binary representations for the weights of all the 1s in the BCD number are added, the result is the Binary number that corresponds to the BCD number.

Code Converters cntd..

Example: Convert the BCD number 0001 0101 (decimal 15) and 1001 0110 (decimal 96) to Binary.

Solution: Write the Binary representations of the weights of all 1s appearing in the numbers, and then add them together

	80	40	20	10	8	4	2	1
Decimal 15	0	0	0	1	0	1	0	1
Decimal 96	1	0	0	1	0	1	1	0

Binary number for Decimal 15 is

```
00000001
00000100
00001010
--------
00001111
--------
```

for 96 is

```
00000010
00000100
00001010
01010000
--------
01100000
--------
```

Code Converters cntd..

EXAMPLE 6–13

(a) Convert the binary number 0101 to Gray code with exclusive-OR gates.

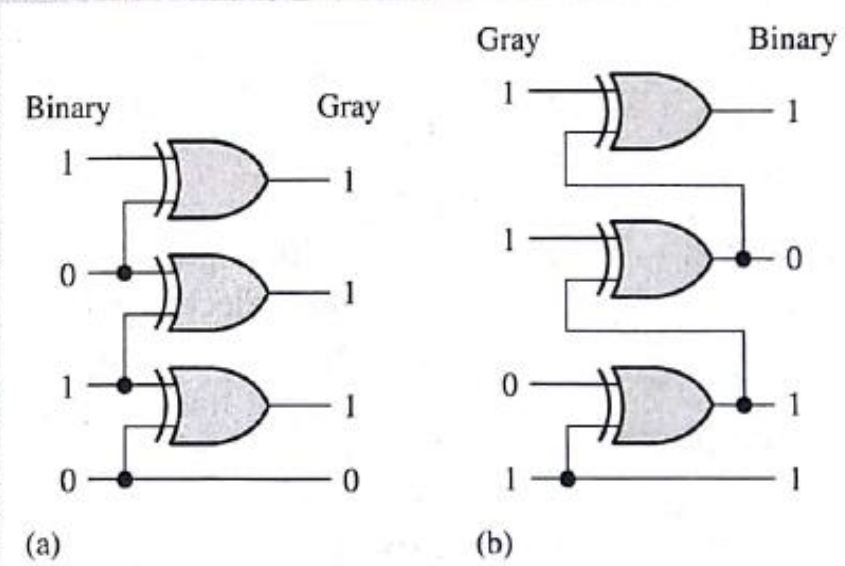
(b) Convert the Gray code 1011 to binary with exclusive-OR gates.

Solution

(a) 0101_2 is 0111 Gray. See Figure 6–45(a).

(b) 1011 Gray is 1101_2. See Figure 6–45(b).

▶ **FIGURE 6–45**



Related Problem How many exclusive-OR gates are required to convert 8-bit binary to Gray?

Multiplexers (Data Selectors)

- A Multiplexer(MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination.
- The basic Multiplexer has several data-input lines and a single output line.
- It also has data select inputs, which permit digital data on any one of the inputs to be switched to the output line
- Multiplexers are also known as Data selectors.
- A logic symbol for a 4 input Multiplexer (MUX) is shown in the Figure 6.49

Multiplexers (Data Selectors) cntd..

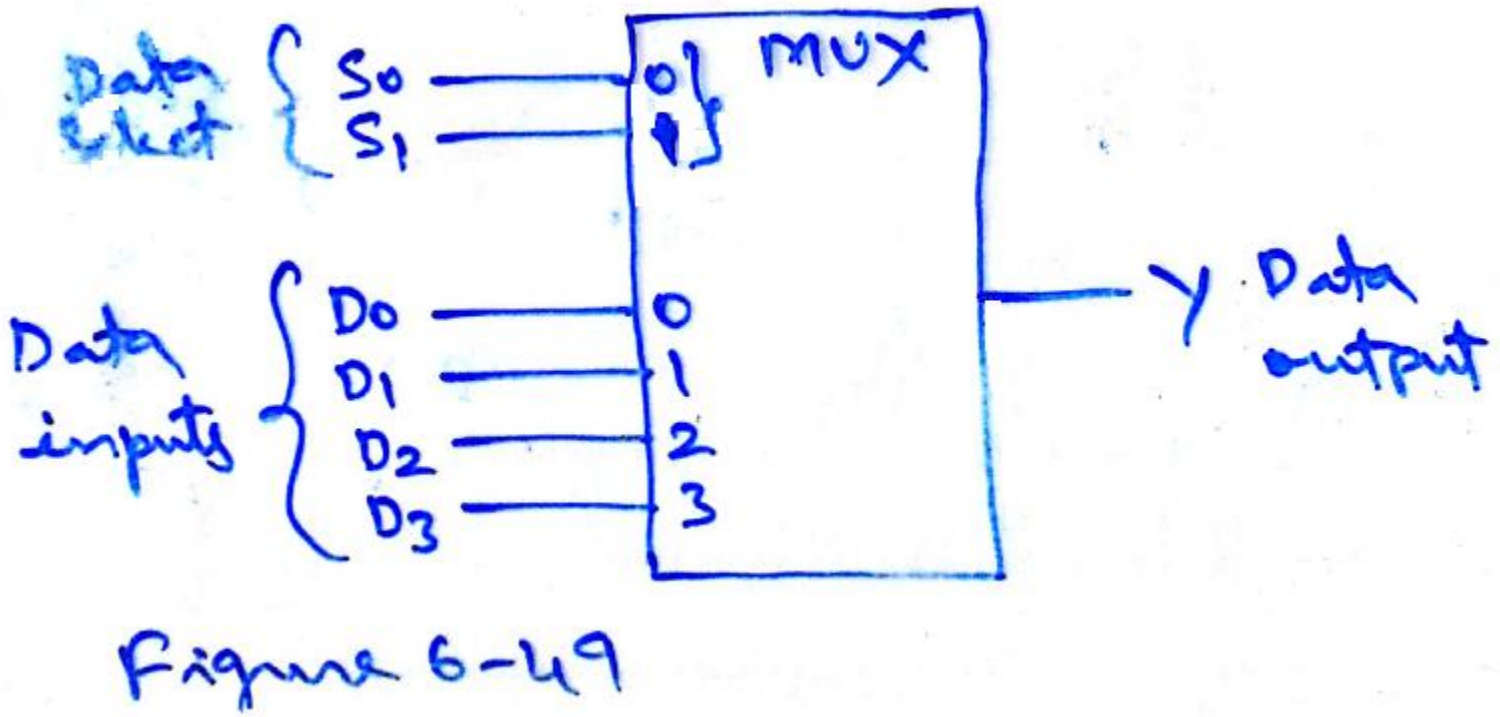


Figure 6-49

Multiplexers (Data Selectors) cntd..

- Notice that there are two data-select lines because with select bits, any one of the four data-input lines can be selected.
- A summary of this selection is shown in table 6.8.

Multiplexers (Data Selectors) cntd..

Data-select Inputs S_1	S_0	Input selected
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Table 6-8

Multiplexers (Data Selectors) cntd..

- Now, let us look at the logic circuiting required to perform this multiplexing operation.
- The data output is equal to the state of the selected data input. You can therefore, derive a logic expression for the output in terms of the data input and the select inputs.

Multiplexers (Data Selectors) cntd..

The data output is equal to D0 only
if S1 =0, and S0=0: $Y = D0\ \overline{S1}\ \overline{S0}$

The data output is equal to D1 only
if S1=0 and S0=1: $Y = D1\ \overline{S1}\ S0$

The data output is equal to D2 only
if S1=1 and S0=0: $Y = D2\ S1\ \overline{S0}$

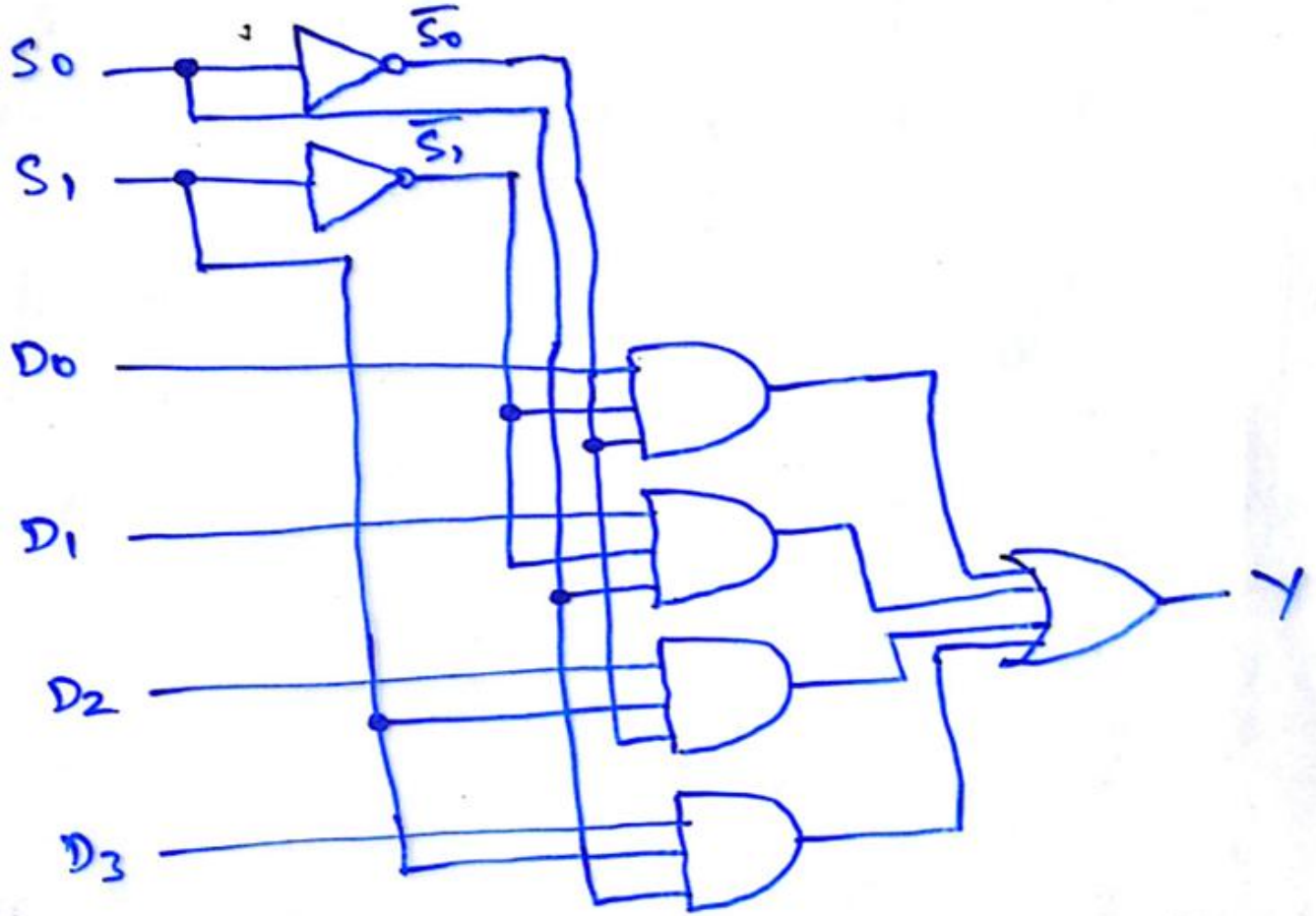
The data output is equal to D3 only
if S1=1 and S0=1: $Y = D3\ S1\ S0$

When these terms are ORed, the total expression for the data output is

$$Y = D0\ \overline{S1}\ \overline{S0} + D1\ \overline{S1}\ S0 + D2\ S1\ \overline{S0} + D3\ S1\ S0$$

The above equation is implemented as shown in Figure 6.47

Multiplexers (Data Selectors) cntd..



6.47

Multiplexers (Data Selectors) cntd..

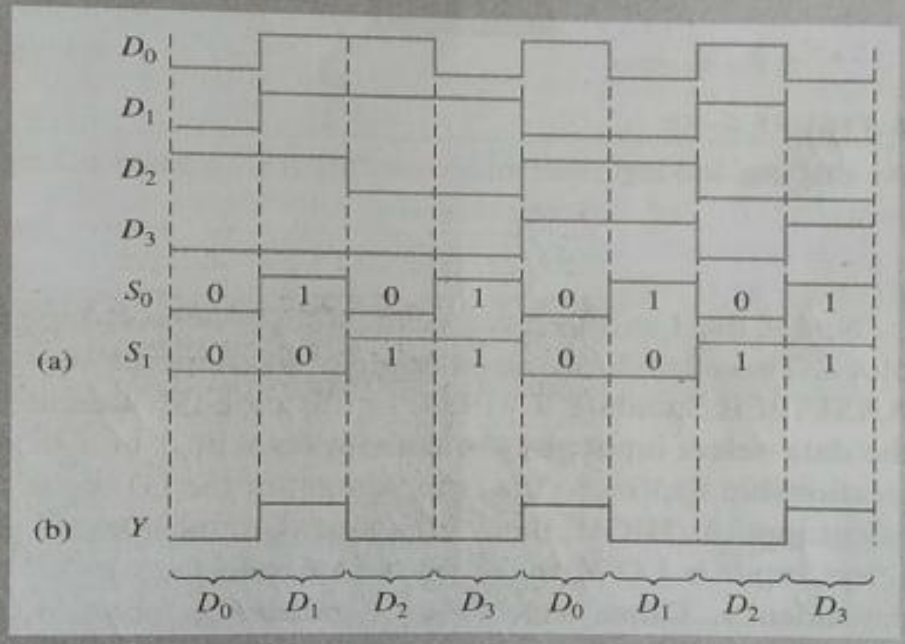
- Because data can be selected from any one of the input lines, this circuit is also referred to as a data selector.

Multiplexers (Data Selectors) cntd..

EXAMPLE 6–14

The data-input and data-select waveforms in Figure 6–48(a) are applied to the multiplexer in Figure 6–47. Determine the output waveform in relation to the inputs.

▶ FIGURE 6–48



Solution The binary state of the data-select inputs during each interval determines which data input is selected. Notice that the data-select inputs go through a repetitive binary sequence 00, 01, 10, 11, 00, 01, 10, 11, and so on. The resulting output waveform is shown in Figure 6–48(b).

Related Problem Construct a timing diagram showing all inputs and the output if the S_0 and S_1 waveforms in Figure 6–48 are interchanged.

An 8-input Data Selector/Multiplexer

- The 74LS151 has eight data inputs (D0 – D7) and, therefore, three data select or address input lines (S0 – S2)
- Three bits are required to select any one of the eight data inputs.
- A LOW on the $\overline{\text{Enable}}$ input allows the selected input data to pass through to the output.
- Notice that the data output and its complement both are available.
- The pin diagram is shown in Figure 6.53a. and the ANSI/IEEE logic symbol is shown in part b.

An 8-input Data Selector/Multiplexer cntd..

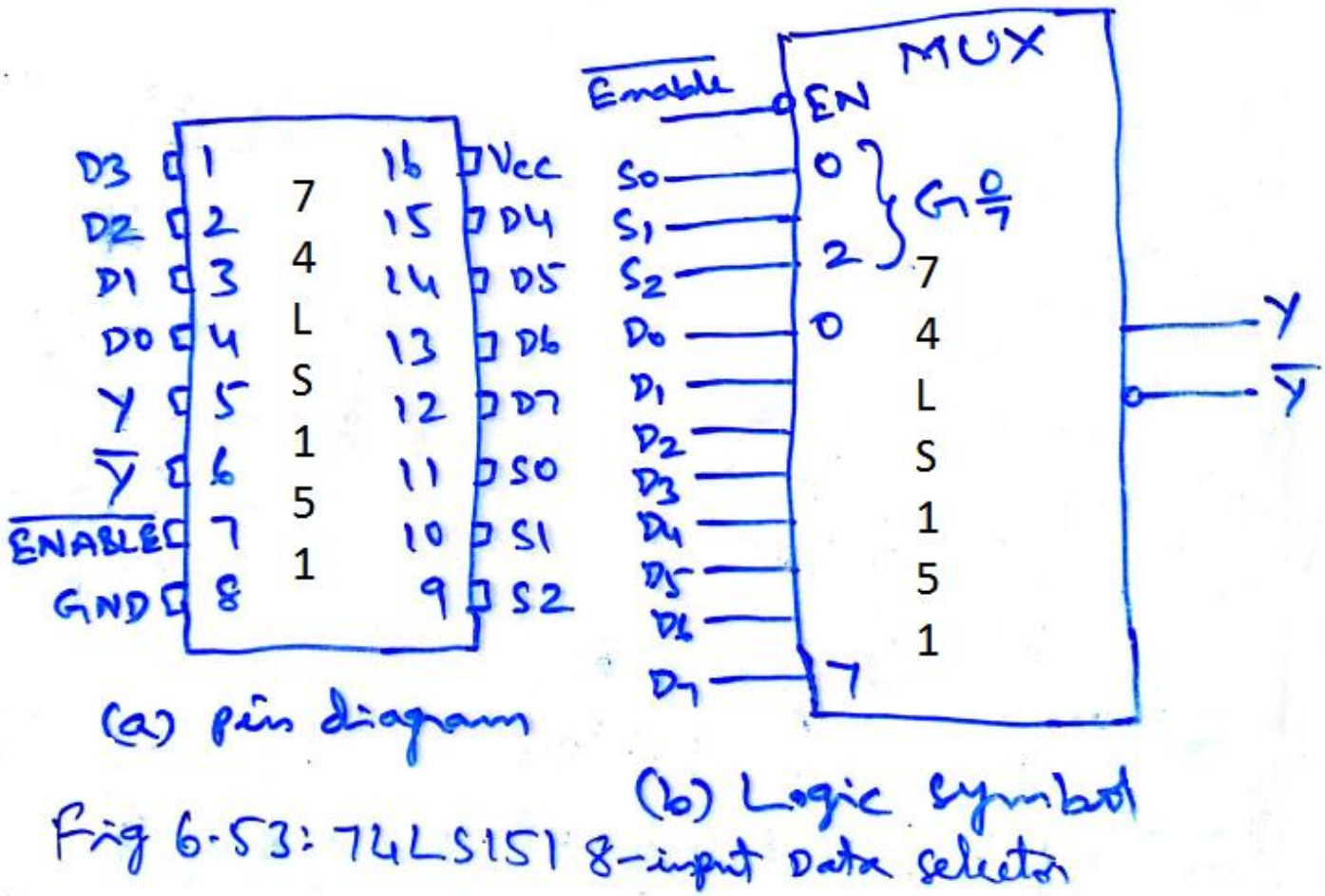


Fig 6.53: 74LS151 8-input Data selector

An 8-input Data Selector/Multiplexer cntd..

- In this case there is no need for a common control block on the logic symbol because there is only one multiplexer to be controlled.
- The G0/7 label with in the logic symbol indicates the AND relationship between the data-select inputs and each of the data inputs 0 through 7.
- Applications of the Multiplexer are
  - 7 segment display multiplexer
  - A logic function generator

Demultiplexers

- A demultiplexer (DEMUX) basically reverses the multiplexing function.
- It takes digital information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor.
- Decoders can also be used as demultiplexers.
- Figure 6.58 shows a 1-line-to-4-line demultiplexer (DEMUX) circuit.
- The data-input line goes to all of the AND gates.
- The two data select lines enable only one gate at a time, and the data appearing on the data input line will pass through the selected gate to the associated data output line.

Demultiplexers cntd..

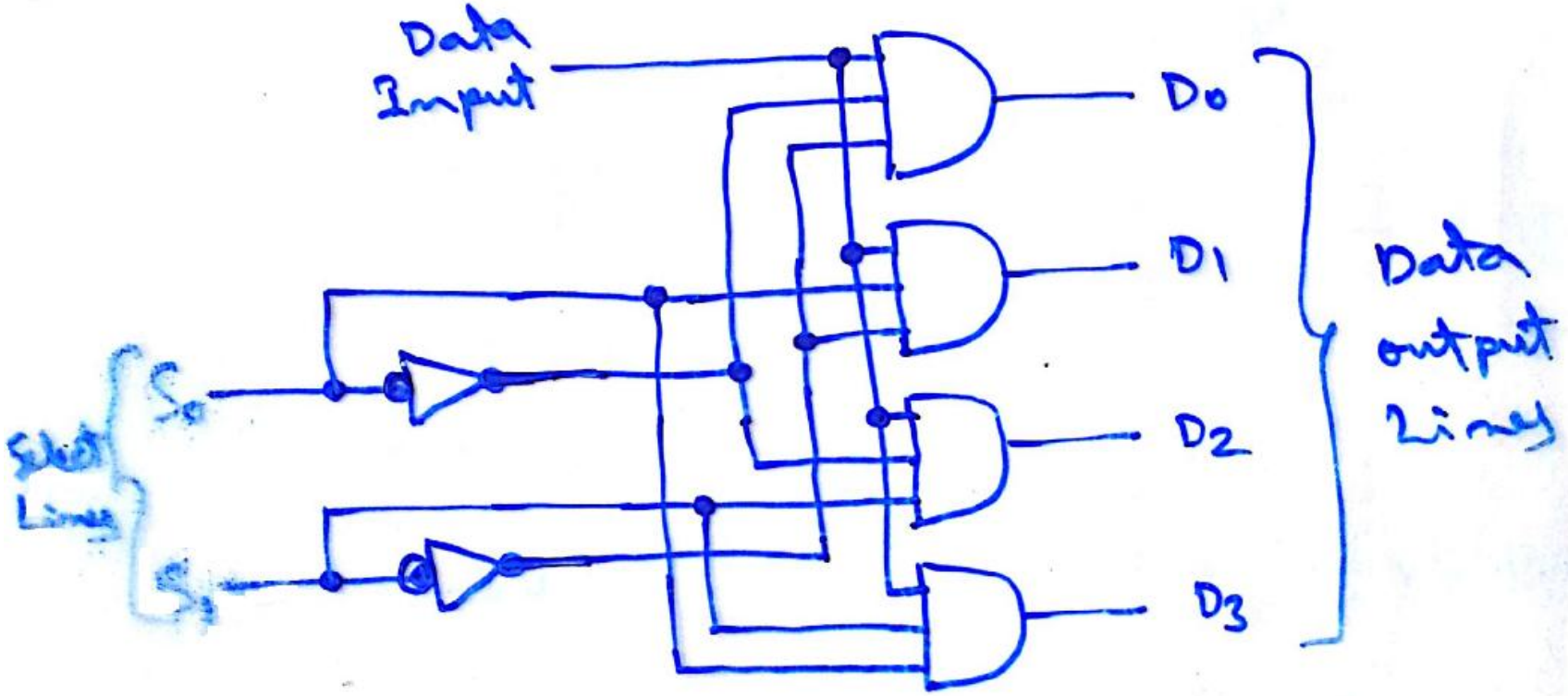


Figure 6-55 1-line-to-4-line DEMUX

Demultiplexers cntd..

- We have already discussed the 74HC154 decoder in its application as a 4-line-to-16-line decoder. This device and other decoders can also be used in demultiplexing applications.
- The logic symbol for this device when used as a demultiplexer is shown in the Figure 6.57.

Demultiplexers cntd..

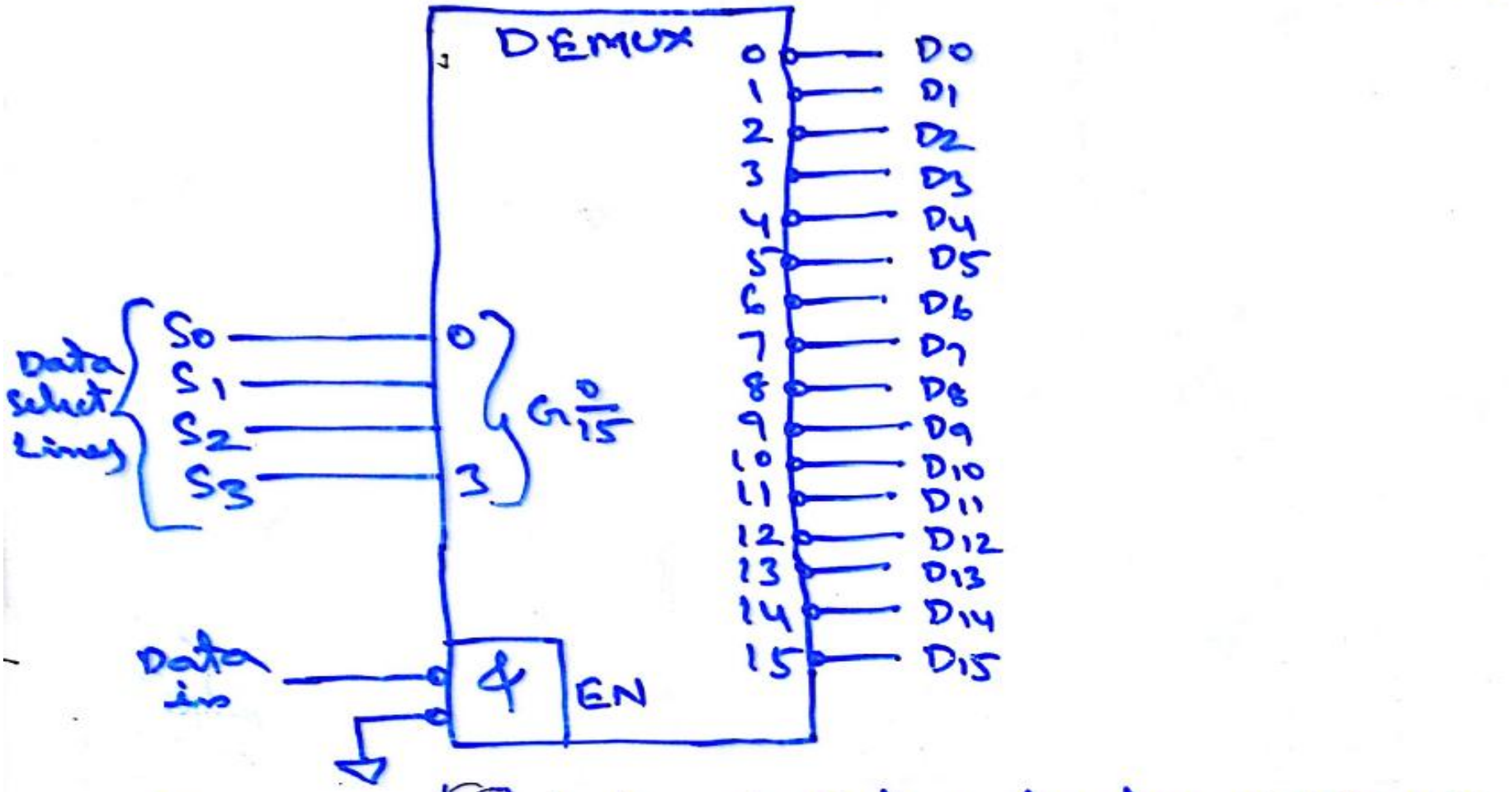


Figure 6 – 4-line-to-16-line decoder as DEMUX.

Demultiplexers cntd..

- In Demultiplexer applications, the input lines are used as the data select lines.
- One of the chip select inputs is used as the data-input line, with the other chip select input held LOW to enable the internal negative-AND gate at the bottom of the diagram.

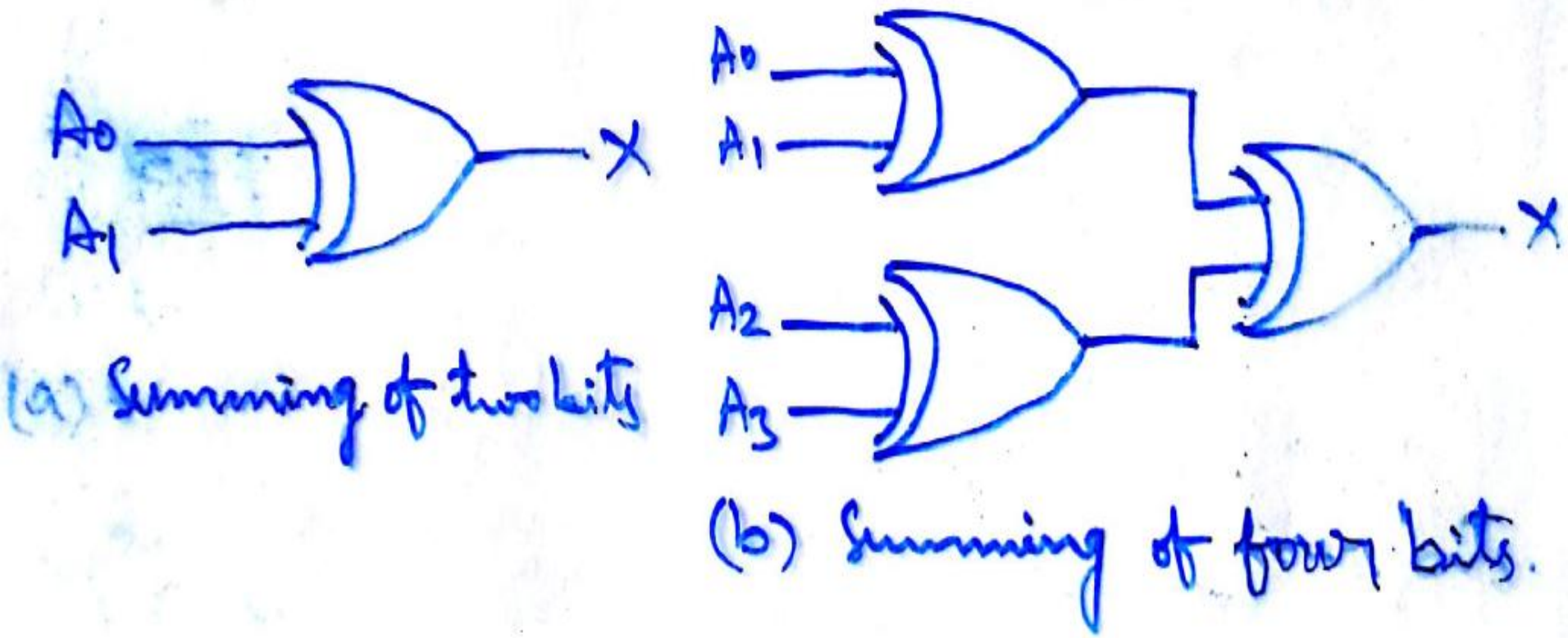
Parity Generators / Checkers

- Errors can occur as digital codes are being transferred from one point to another with in a digital system or white codes are being transmitted from system to another.
- The errors take the form of undesired changes in the bits that make up the coded information; that is, a 1 can change to a 0, or a 0 to a 1, because of component malfunctions or electrical noise.
- In most digital systems, the probability that even a single bit error will occur is very small, and the likelihood that more than one will occur is even smaller. Nevertheless, when an error occurs undetected, it can cause serious problems in a digital system.

Parity Generators / Checkers cntd..

- In order to check for or to generate the proper parity in a given code, a basic principle can be used :
  - The sum (disregarding carries) of an even number of 1s is always 0, and the sum of an odd number of 1s is always 1.
- Therefore, to determine if a given code has even parity or odd parity, all the bits in that code are summed.
- The sum of two bits can be generated by an exclusive – OR gate, as shown in the Figure 6.61a.; the sum of 4 bits can be formed by three exclusive-OR gates connected as shown in Figure 6.61b; and so on.

Parity Generators / Checkers cntd..



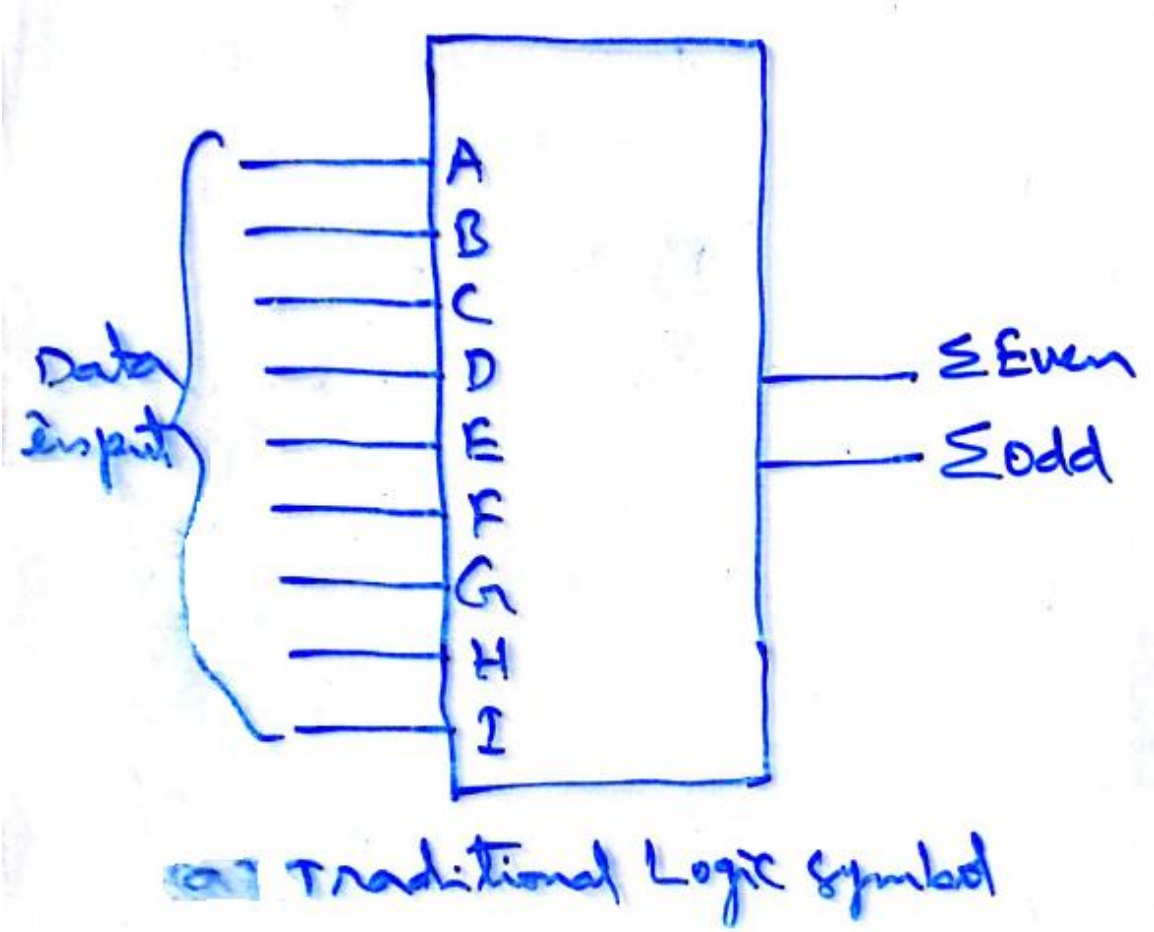
Parity Generators / Checkers cntd..

- When the number of 1s on the inputs is even, the output X is 0 (LOW). When the number of 1s is odd, the output X is 1(HIGH).

A 9 bit Parity Generator / Checker

- The logic symbol and function table for a 74LS280, are shown in Figure 6.62.

Parity Generators / Checkers cntd..



(a) Traditional Logic symbol

Parity Generators / Checkers cntd..

Number of Inputs A-I that are HIGH	outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

(b) function table

Figure 6-62.

Parity Generators / Checkers cntd..

- This particular device can be used to check for odd or even parity on a 9-bit code (eight data bits and one parity bit) or it can be used to generate a parity bit for a binary code with up to nine bits.
- The inputs are A through I; when there is an even number of 1s on the inputs, the $\Sigma EVEN$ output is HIGH and the ΣODD output is LOW.

Parity Generators / Checkers cntd..

Parity Checker:

- When this device is used as an even parity checker, the number of input bits should always be even; and when a parity error occurs, the $\Sigma EVEN$ output goes LOW and the ΣODD output goes HIGH.
- When it is used as an odd parity checker, the number of input bits should always be odd; and when a parity error occurs, the ΣODD output goes LOW and the $\Sigma EVEN$ output goes HIGH.

Parity Generators / Checkers cntd..

Parity Generator:

- If this device is used as an even parity generator, the parity bit is taken as the ΣODD output because this output is a 0 if there is an even number of input bits and it is a 1 if there is an odd number.
- When used as an odd parity generator, the parity bit is taken as the $\Sigma EVEN$ output, because it is a 0 when the number of input bits is odd.

End of Unit IV

Unit V

Sequential Logic ICs and Memories

Flip-Flops

- Latches and Flip-flops are almost similar type of devices but the main difference between them is in the method used for changing their state.
- Flip-flops are synchronous bi-stable devices, also known as bi-stable multivibrators
- In this case, the term synchronous means that the output changes state only at a specified point on the triggering input called the clock (CLK), which is designated as a control input, ie changes in the output occur in synchronization with the clock.

Flip-flops cntd..

- An edge-triggered Flip-flop changes state either at the positive edge(raising edge) or at the negative edge(falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.
- Three types of edge-triggered Flip-flops are shown in the figure 7.13.

Flip-flops cntd..

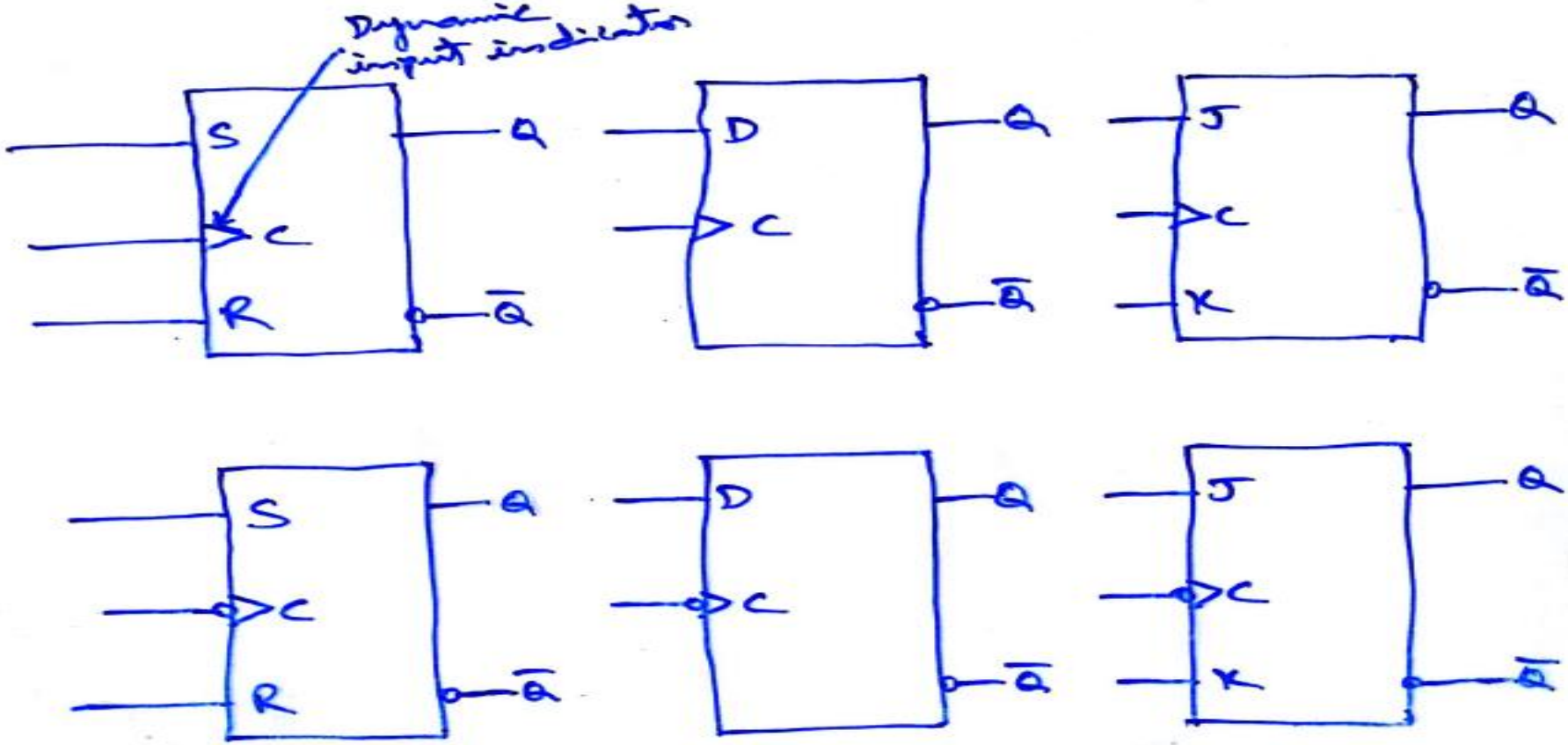


Fig 7-13 (a) S-R (b) D (c) J-K

Edge triggered flip-flop logic symbols

Flip-flops cntd..

- Although the S-R flip-flop is not available in IC form, it is the basis for the D and J-K flip-flops.
- Notice that each type can be either positive edge triggered (no bubble at C input) or negative edge triggered (bubble at C input).
- The key to identifying an edge triggered flip-flop by it's logic symbol is the small triangle inside the block at the clock (C) input.
- This triangle is called the dynamic input indicator. The dynamic input indicator, > (Symbol), means the flip-flop changes the state only on the edge of a clock pulse.

The Edge Triggered S-R Flip-flop

- The S and R inputs of the S-R flip-flop are called synchronous inputs because data on these inputs are transferred to the flip-flops output only on the triggering edge of the clock pulse.
- The basic operation of a positive edge-triggered flip-flop is illustrated in Figure 7.14 and table 7.2 is the truth table for this type of flip-flop.

The Edge Triggered S-R Flip-flop cntd..

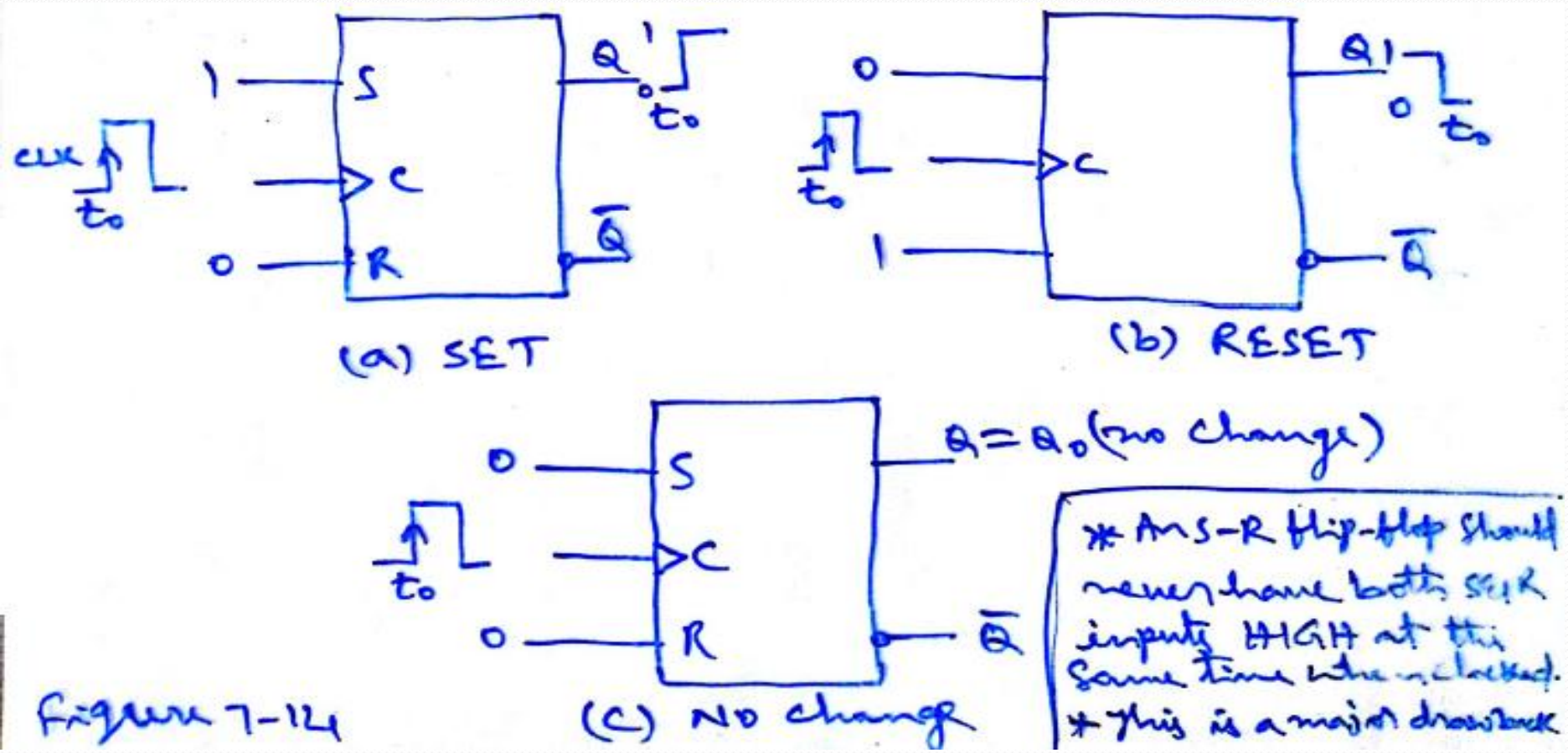


Figure 7-14

The Edge Triggered S-R Flip-flop cntd..

INPUTS			OUTPUTS		COMMENTS
S	R	CLK	Q	$\overline{Q}$	
0	0	X	Q_0	$\overline{Q_0}$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

↑ = clock transition (LOW to HIGH)

Table 7-2 Truth table for a +ve edge-triggered S-R flip-flop.

The Edge Triggered S-R Flip-flop cntd..

- The operation and truth table for a negative edge triggered S-R flip-flop are the same as those for a positive edge triggered device except that the falling edge of the clock pulse is the triggering edge.

Example 1:

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7.15 for the S, R, and CLK inputs in the Figure 7.16a. Assume that the positive edge triggered flip-flop is initially RESET.

The Edge Triggered S-R Flip-flop cntd..

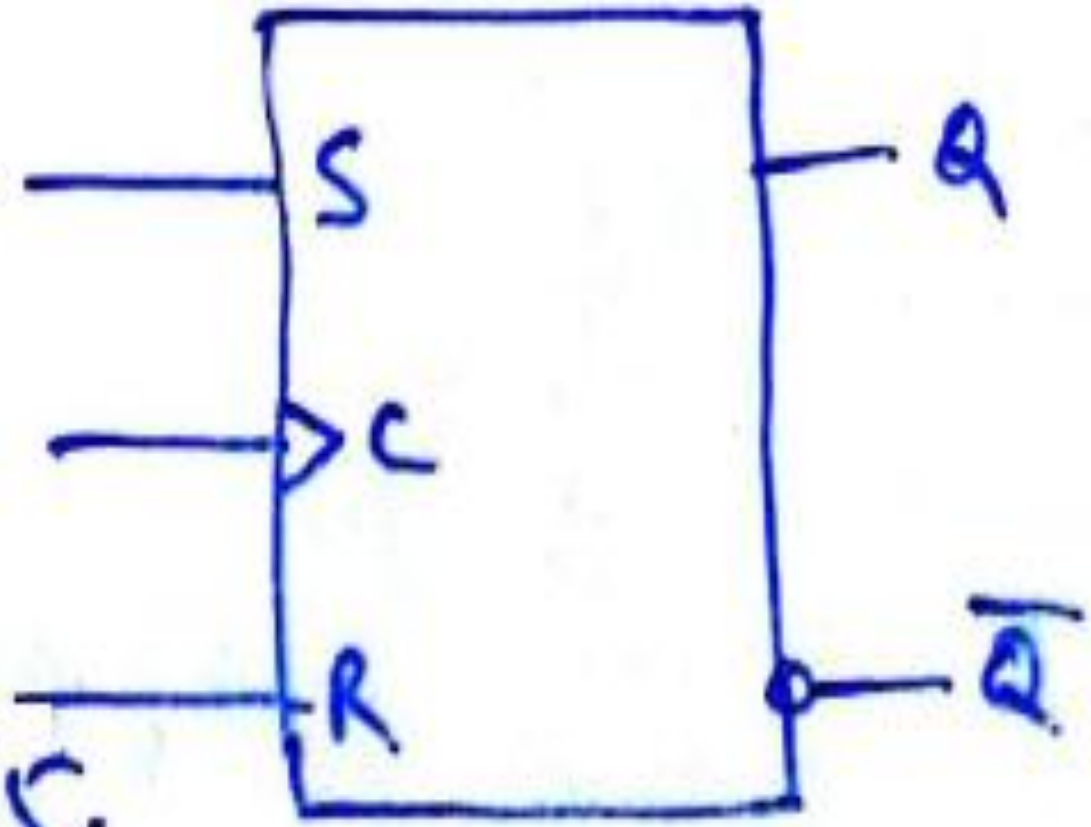


Figure 7-15.

The Edge Triggered S-R Flip-flop cntd..

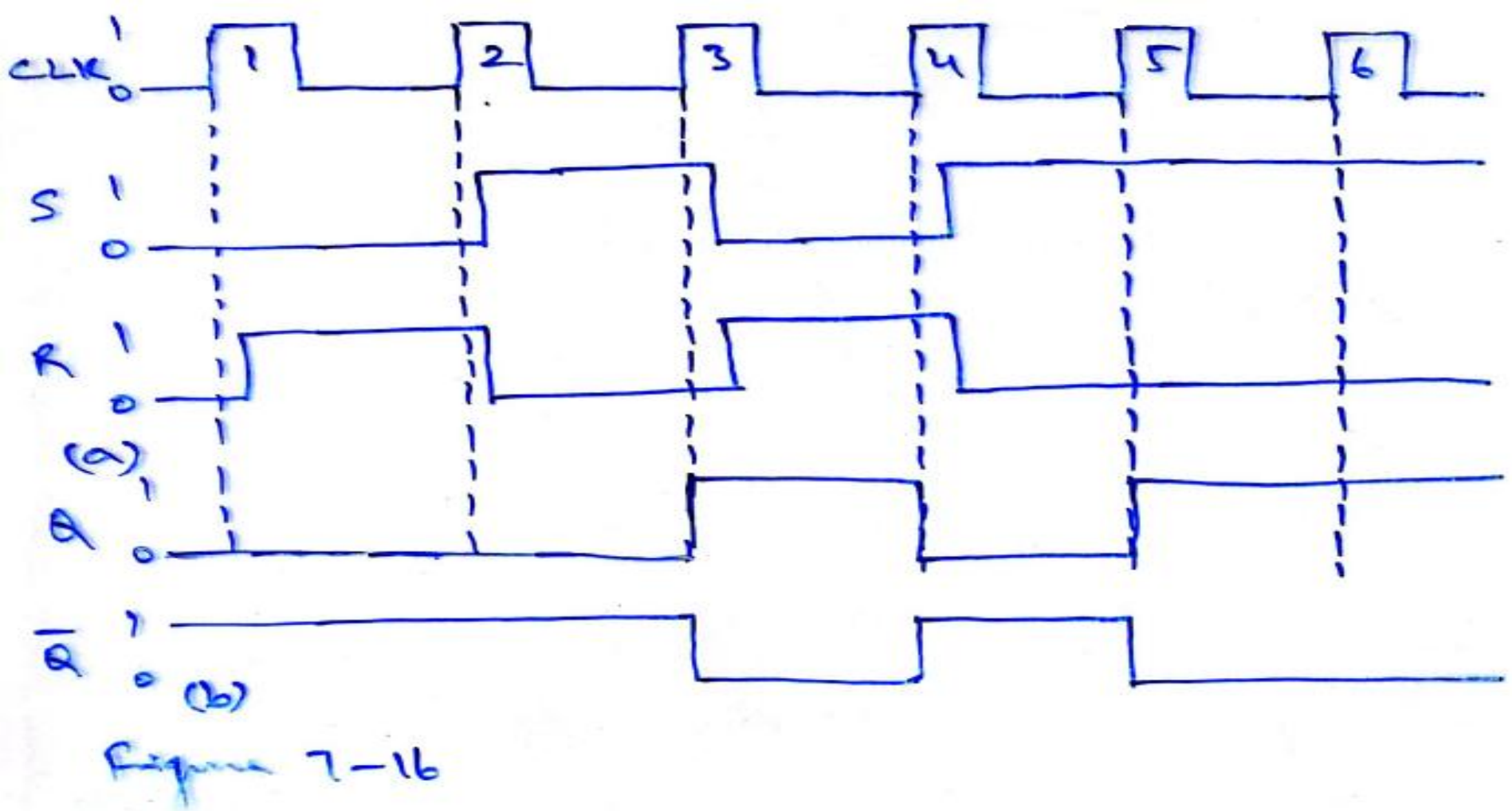


Figure 7-16

The Edge Triggered S-R Flip-flop cntd..

Home Work 1: Determine Q and $\overline{Q}$ for the S and R inputs in Figure 7.16a if the flip-flop is a negative edge triggered device.

The Edge triggered D Flip-flop

- The D flip-flop is useful when a single data bit (1 or 0) is to be stored.
- The addition of an inverter to an S-R flip-flop creates a basic D flip-flop, as in Figure 7.20, where a positive edge triggered type is shown.

The Edge triggered D Flip-flop cntd..

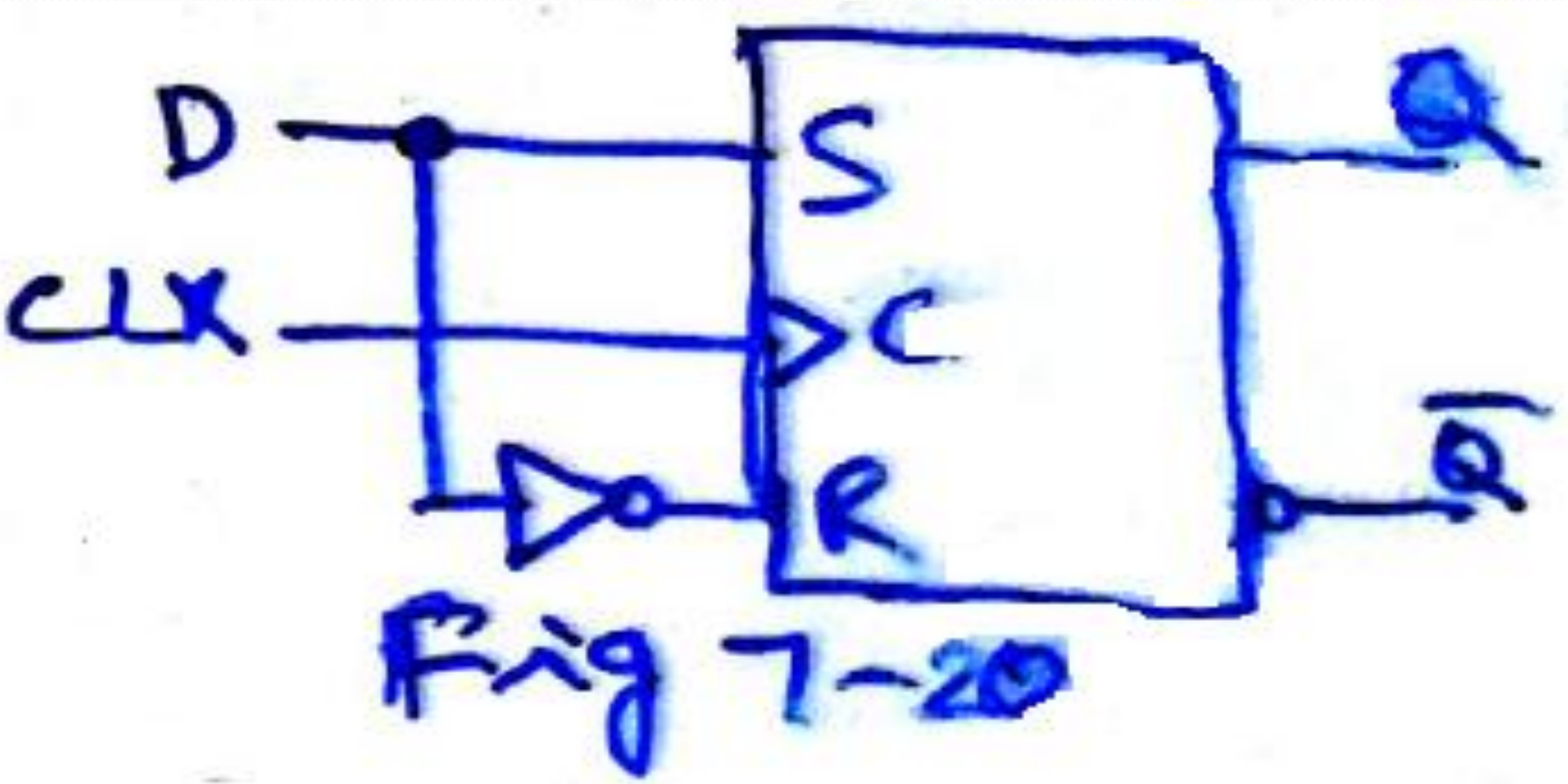


Fig 7-20

The Edge triggered D Flip-flop cntd..

- Notice that the flip-flop in Figure 7.20 has only one input, the D input, in addition to the clock.
- The logical operation of the positive edge triggered D flip-flop is summarized in table 7.3.

The Edge triggered D Flip-flop cntd..

INPUTS D	INPUTS CLK	OUTPUTS Q	OUTPUTS $\bar{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

Table 7-3: Truth table for a positive edge-triggered D flip-flop.

The Edge triggered D Flip-flop cntd..

- The operation of a negative edge triggered device is, of course, the same, except that triggering occurs on the falling edge of the clock pulse.
- Remember, Q follows D at the active or triggering clock edge.

Example 2:

Given the waveforms in Figure 7.21a for the D input and the clock, determine the Q output waveform if the flip-flop starts at RESET.

The Edge triggered D Flip-flop cntd..

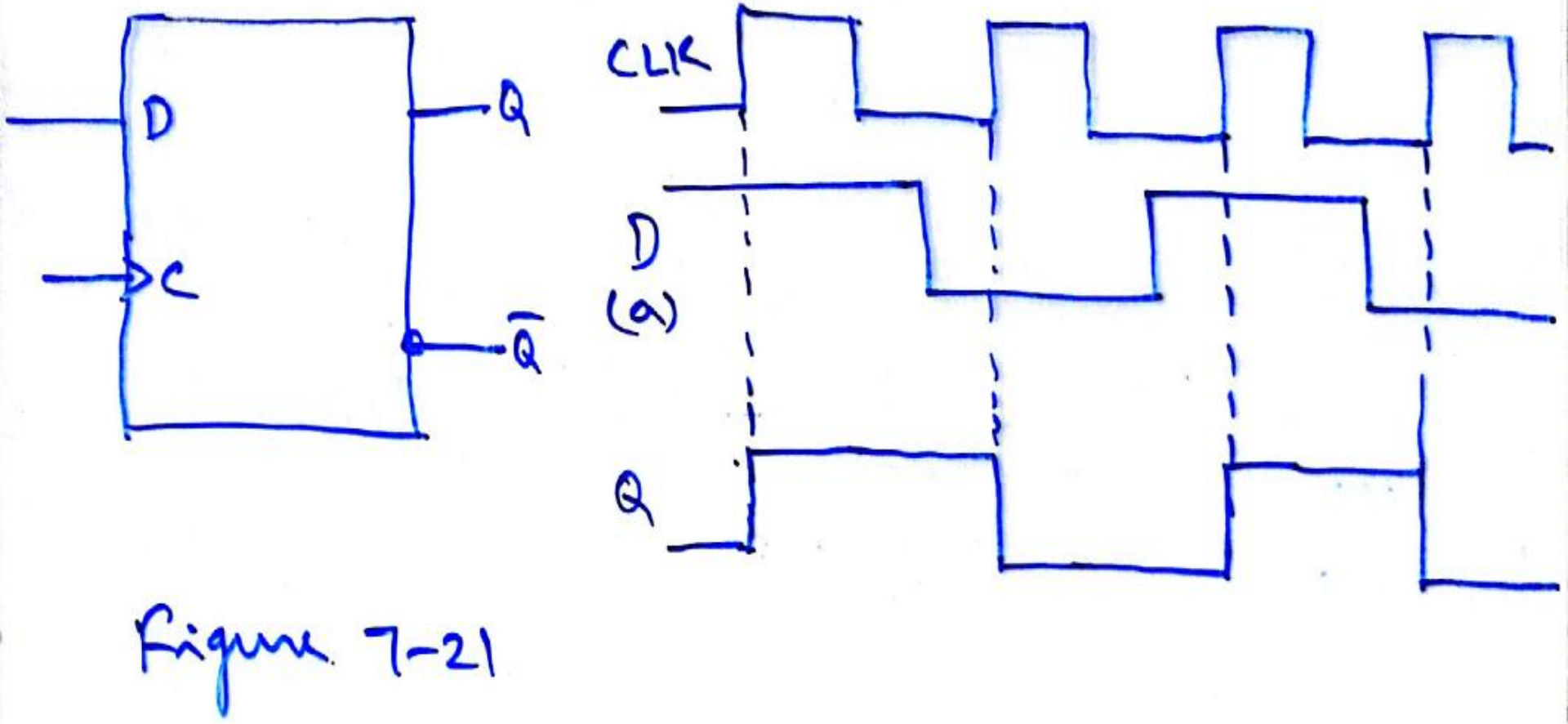


Figure 7-21

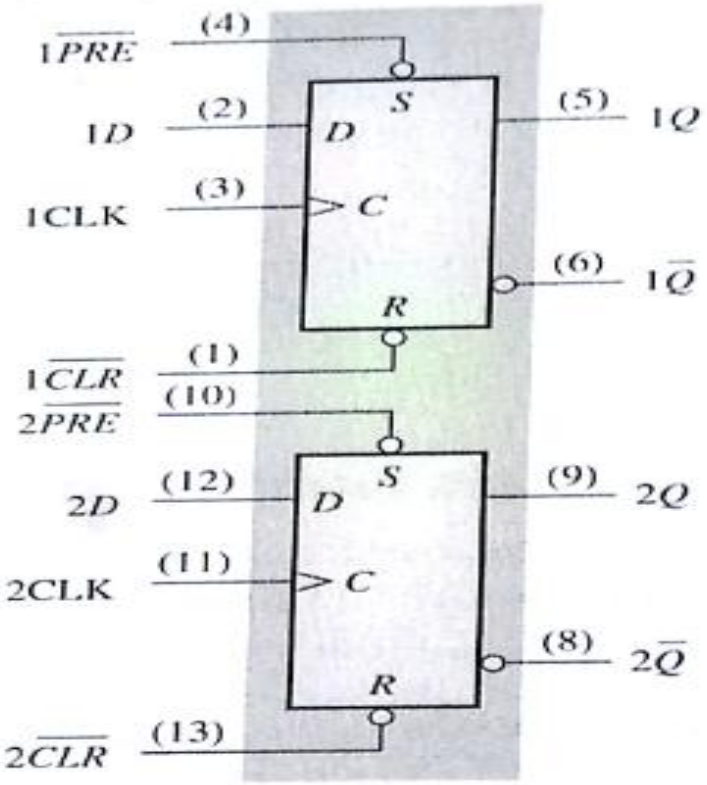
The Edge triggered D Flip-flop cntd..

Home Work 2: Determine the Q output for the D flip-flop if the D input in the figure 7.21a is inverted.

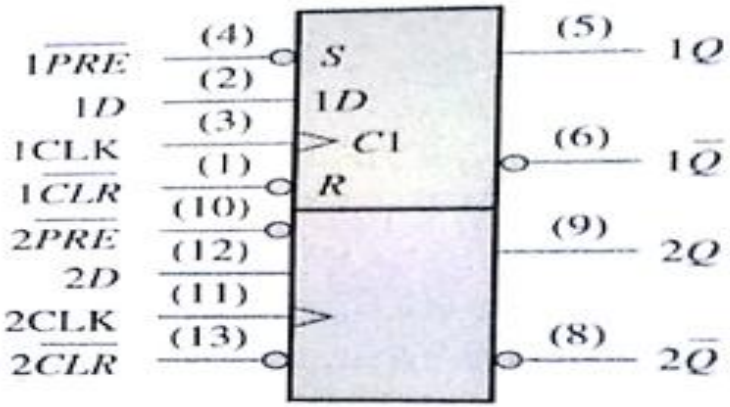
The 74AHC74 Dual D Flip-flop

- This device contains two identical D flip-flops that are independent of each other except for sharing Vcc and Ground.
- The flip-flops are positive edge-triggered and have active LOW asynchronous preset and clear inputs.
- The logic symbols for the individual flip-flops within the package are shown in Figure 7.29a, and an ANSI/IEEE standard single block symbol that represents the entire device is shown in part (b). The pin numbers are shown in parenthesis.

The 74AHC74 Dual D Flip-flop cntd..



(a) Individual logic symbols



(b) Single block logic symbol
Note: The S and R inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS.

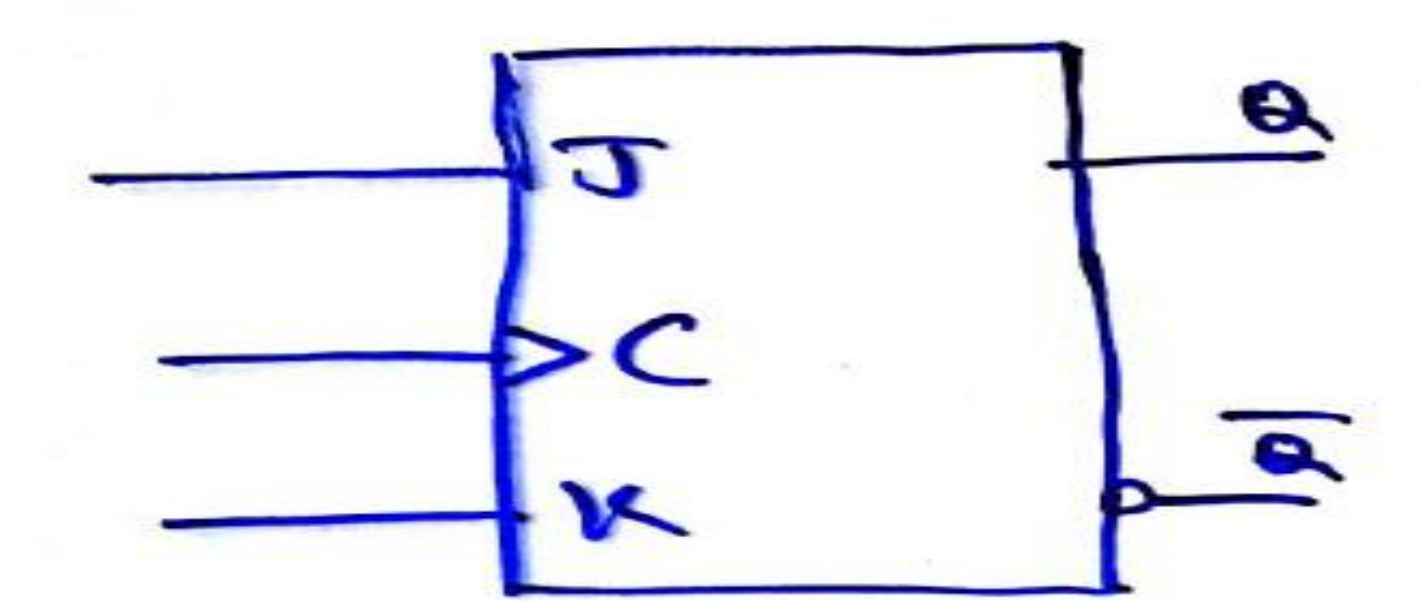
▲ FIGURE 7–29

Logic symbols for the 74AHC74 dual positive edge-triggered D flip-flop.

The Edge triggered JK Flip-flop

- The JK flip-flop is versatile and is a widely used type of flip-flop.
- The functioning of the JK flip-flop is identical to that of the SR flip-flop in the SET, RESET, and no-change conditions of operation. The difference is that the JK flip-flop has no invalid state as does the SR flip-flop.
- Figure 7.22 shows the JK flip-flop and the basic internal logic for a positive edge triggered JK flip-flop.

The Edge triggered JK Flip-flop cntd..



(a) J-K flip-flop

Fig 7-22

The Edge triggered JK Flip-flop cntd..

- The two control inputs are labeled J and K in the honor of Jack Kilby, who invented the IC.
- A JK flip-flop can also be of the negative edge triggered type, in which case the clock input is inverted.
- Table 7.4 summarizes the logical operation of the edge triggered JK flip-flop in the truth table form.

The Edge triggered JK Flip-flop cntd..

INPUTS			OUTPUTS		COMMENTS
J	K	CLK	Q	$\bar{Q}$	
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

Table 7-4 Truth table for a +ve edge-triggered JK flip-flop

The Edge triggered JK Flip-flop cntd..

- Notice that there is no invalid state as there is with an SR filp-flop. It is the toggle state.
- A JK flip-flop connected for toggle operation is sometimes called a T flip-flop.
- The truth table for a negative edge triggered device is identical except that it is triggered on the falling edge of the clock pulse.

Example 3: The waveforms in Figure 7.24a are applied to the J,K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

The Edge triggered JK Flip-flop cntd..

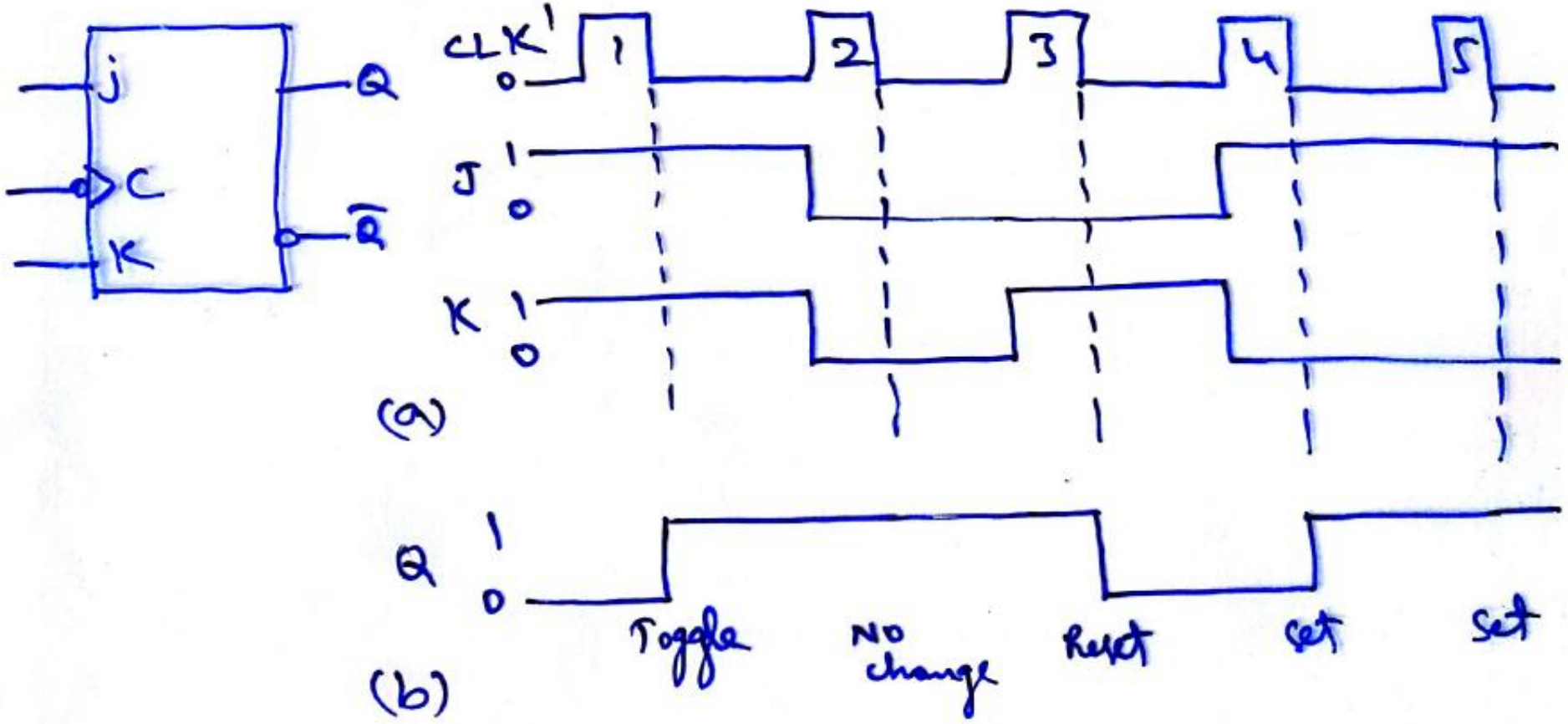


Fig 7-24

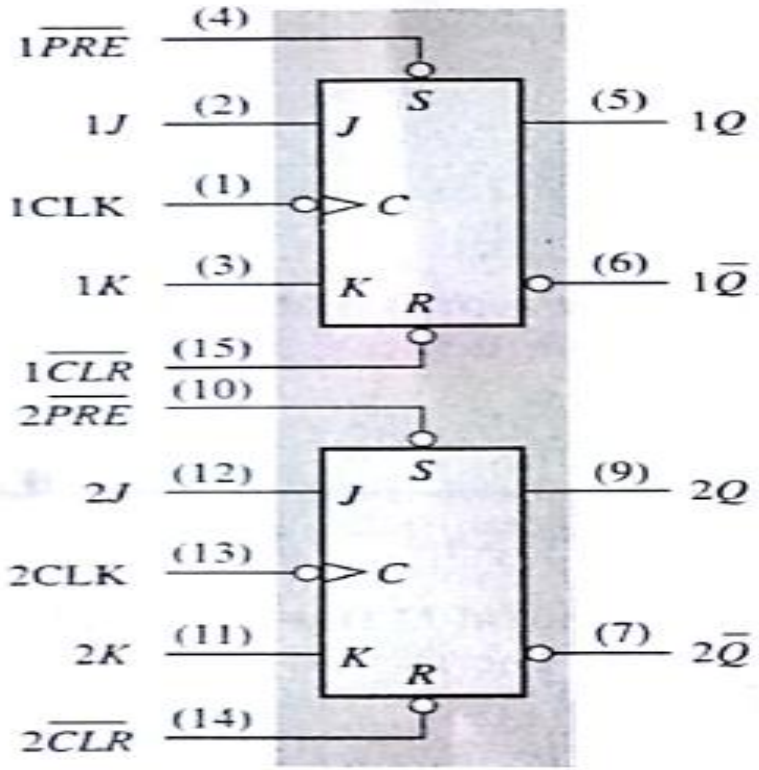
The Edge triggered JK Flip-flop cntd..

Home Work 3: Determine the Q output of the JK flip-flop if the J and K inputs in Figure 7.24a are inverted.

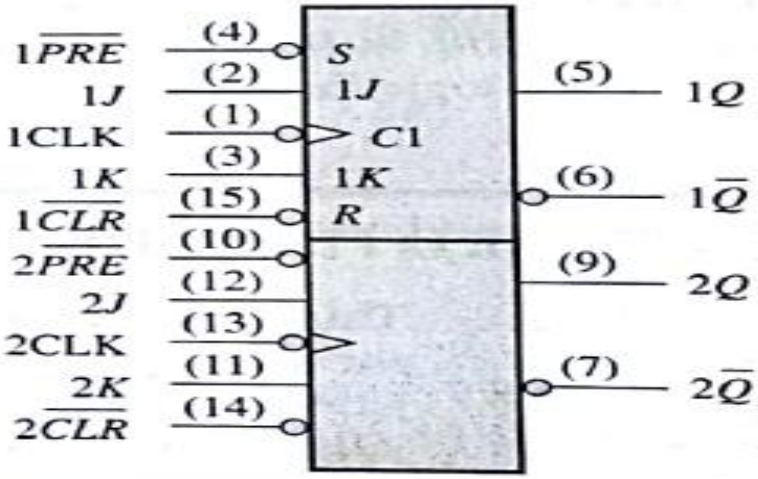
The 74HC112 Dual JK Flip-flop

- This device has two identical flip-flops that are negative edge triggered and have active LOW asynchronous preset and clear inputs.
- The logic symbols are shown in Figure 7.30.

The 74HC112 Dual JK Flip-flop cntd..



(a) Individual logic symbols



(b) Single block logic symbol

▲ FIGURE 7–30

Logic symbols for the 74HC112 dual negative edge-triggered J-K flip-flop.

Conversion of Flip-flops

The following steps indicate the procedure to be followed to convert a flip-flop into another flip-flop.

Steps:

1. Identify available and required flip-flops.
2. Make characteristics table for the required flip-flop.
3. Make excitation table for available flip-flop.
4. Write boolean expression for available flip-flop.
5. Draw the circuit.

JK to D flip-flop conversion

1) Identify available and required flip-flop

available flip-flop = JK

required flip-flop = D

JK to D flip-flop conversion cntd..

2) make characteristic table for required FF (D)

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

3) make excitation table for available FF

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_n	D	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

JK to D flip-flop conversion cntd..

4) write boolean expressions for available Flip-flop

for J

Q_n \ D	0	1
0	0	1
1	x	x

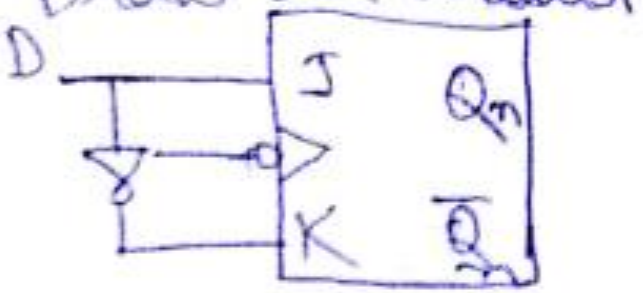
$J = D$

for K

Q_n \ D	0	1
0	x	x
1	1	0

$K = \overline{D}$

5) Draw the circuit



T flip-flop to D flip-flop conversion

T Flip-flop to D Flip-flop Conversion ③

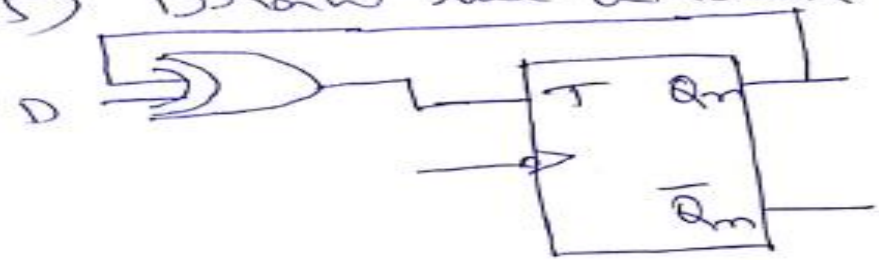
1) Identify available and required flip-flop.
   available FF = T
   Required FF = D

2),3) Make characteristic table for required FF and make excitation table for available FF

Qn	D	Qn+1	T
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

4) Boolean expression is
   $T = D \oplus Q_n$

5) Draw the circuit



SR Flp-flop to JK Flip-flop conversion

1) Available flip-flop = SR

   Required flip-flop = JK

SR Flp-flop to JK Flip-flop conversion cntd..

2) make characteristics table for required FF.

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

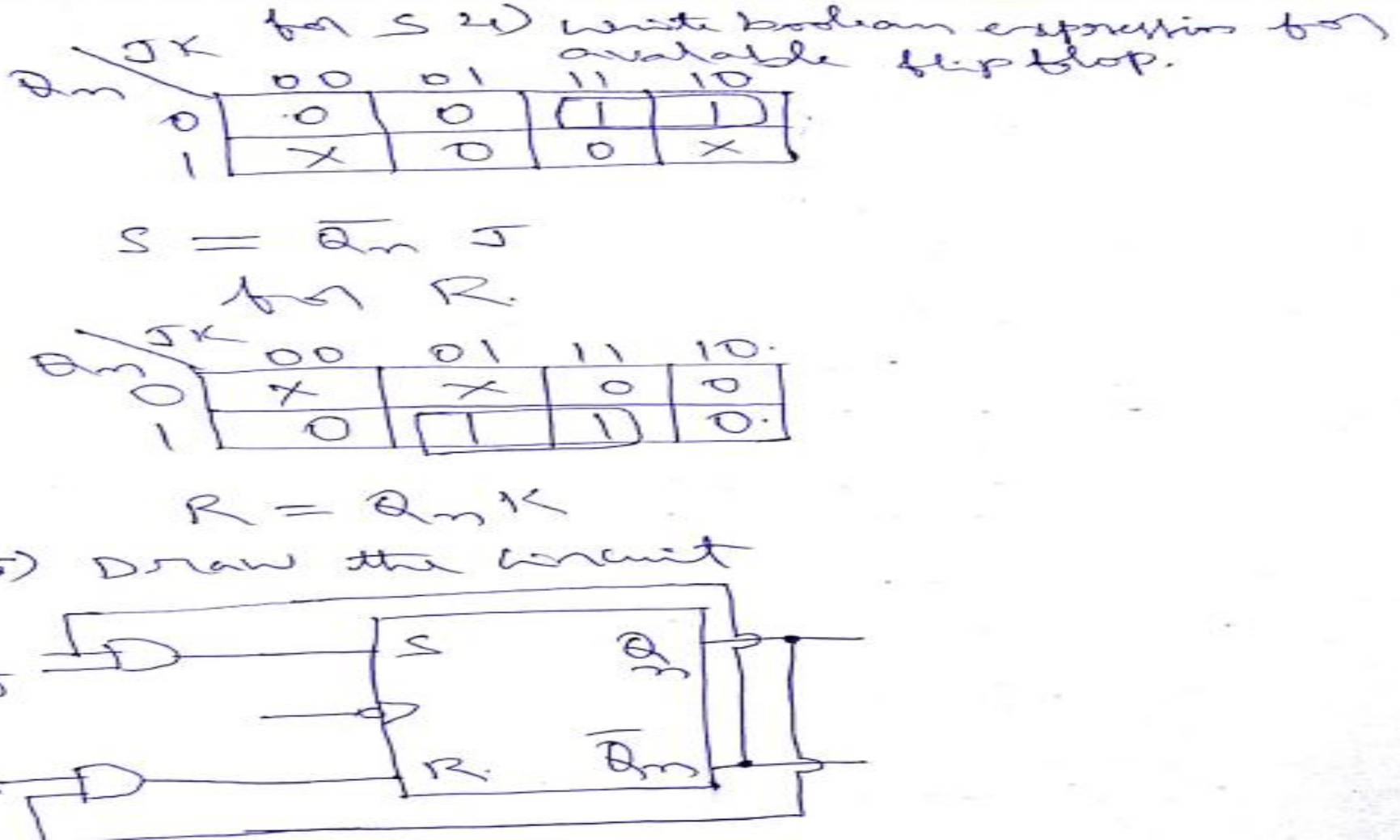
SR Flp-flop to JK Flip-flop conversion cntd..

3) make excitation table for available FF

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_n	J	K	Q_{n+1}	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

SR Flp-flop to JK Flip-flop conversion cntd..



SR flip-flop to T flip-flop conversion

1) Identify available flip-flop and required flip-flop

Available flip-flop = SR

Required flip-flop = T

SR flip-flop to T flip-flop conversion cntd..

2) make characteristic table for required FF

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

3) make excitation table for ~~SR~~ available FF (SR)

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_n	T	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	X	0
1	1	0	0	1

SR flip-flop to T flip-flop conversion cntd..

4) Write boolean expressions for available FF

For S

Q_n \ T	0	1
0	0	(1)
1	X	0

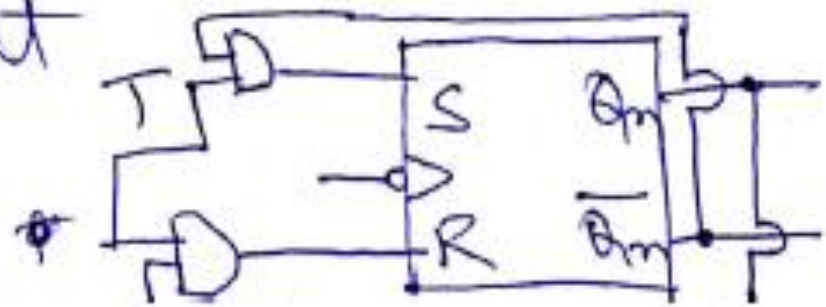
$S = \overline{Q_n} T$

for R

Q_n \ T	0	1
0	X	0
1	0	(1)

$R = Q_n T$

5) Draw the circuit



SR flip-flop to D flip-flop conversion cntd..

Home Work: Convert SR flip-flop to D flip-flop.

Counters

- Counters are classified into two broad categories according to the way they are clocked; asynchronous and synchronous.
- In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop.
- In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.
- With in each of these two categories, counters are classified primarily by the type of sequence, the number of states, or the number of flip-flops in the counter.

Memories

There are two types of Memories.

1. ROM 2. RAM

ROM: The Read Only Memory

- A ROM contains permanently or semi-permanently stored data, which can be read from the memory but either can not be changed at all or cannot be changed with out specialized equipment.
- A ROM stores data that are used repeatedly in system applications, such as tables, conversions, or programmed instructions for system initialization and operation.
- ROMs retain stored data when the power is off and are therefore non-volatile memories.

Memories cntd..

The ROM Family:

- Figure 10.22 shows how semiconductor ROMs are categorized.

Memories cntd..

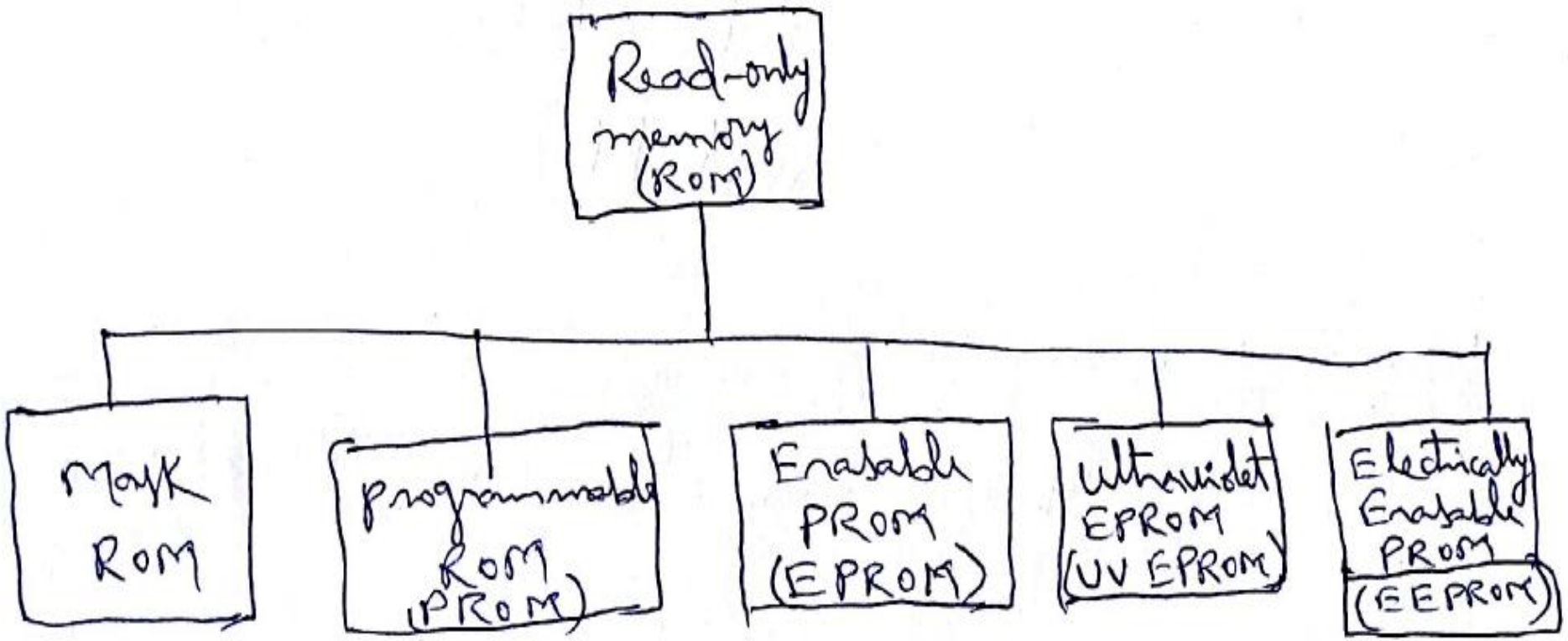


Fig 10-22 The ROM family

Memories cntd..

- the mask ROM is the type in which the data are permanently stored in the memory during the manufacturing process.
- The PROM, or Programmable ROM, is the type in which the data are electrically stored by the user with the aid of specialized equipment.
- Both the mask ROM and the PROM can be of either MOS or bipolar technology.

Memories cntd..

- The EPROM, or erasable PROM, is strictly a MOS device.
- The UVEPROM is electrically programmable by the user, but the stored data must be erased by exposure to ultraviolet light over a period of several minutes.
- The electrically erasable PROM (EEPROM or E^2PROM) can be erased in a few milliseconds.

Memories cntd..

The Random Access Memory (RAM)

- A RAM is a read/write memory in which data can be written into or read from any selected address in any sequence.
- When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new data unit.
- When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation.

Memories cntd..

- A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off.
- The two major categories of RAM are the static RAM (SRAM) and the dynamic RAM (DRAM).
- SRAMs generally use latches as storage elements and can therefore store data indefinitely as long as dc power is applied.
- DRAMs use capacitors as storage elements and cannot retain data very long without the capacitors being recharged by a process called refreshing.
- Both SRAMs and DRAMs will lose stored data when DC power is removed and therefore, are classified as volatile memories.

Memories cntd..

- Data can be read much faster from SRAMs than from DRAMs.
- However, DRAMs can store much more data than SRAMs for a given physical size and cost because the DRAM cell is much simpler, and more cells can be crammed into a given chip area than in the SRAM.
- The basic types of SRAM are the asynchronous SRAM and the synchronous SRAM with a burst feature.
- The basic types of DRAM are the fast page mode DRAM (FPM DRAM), the Extended Data Out DRAM (EDO DRAM), the Burst EDO DRAM (BEDO DRAM), the synchronous DRAM (SDRAM). These are shown in figure 10.7.

Memories cntd..

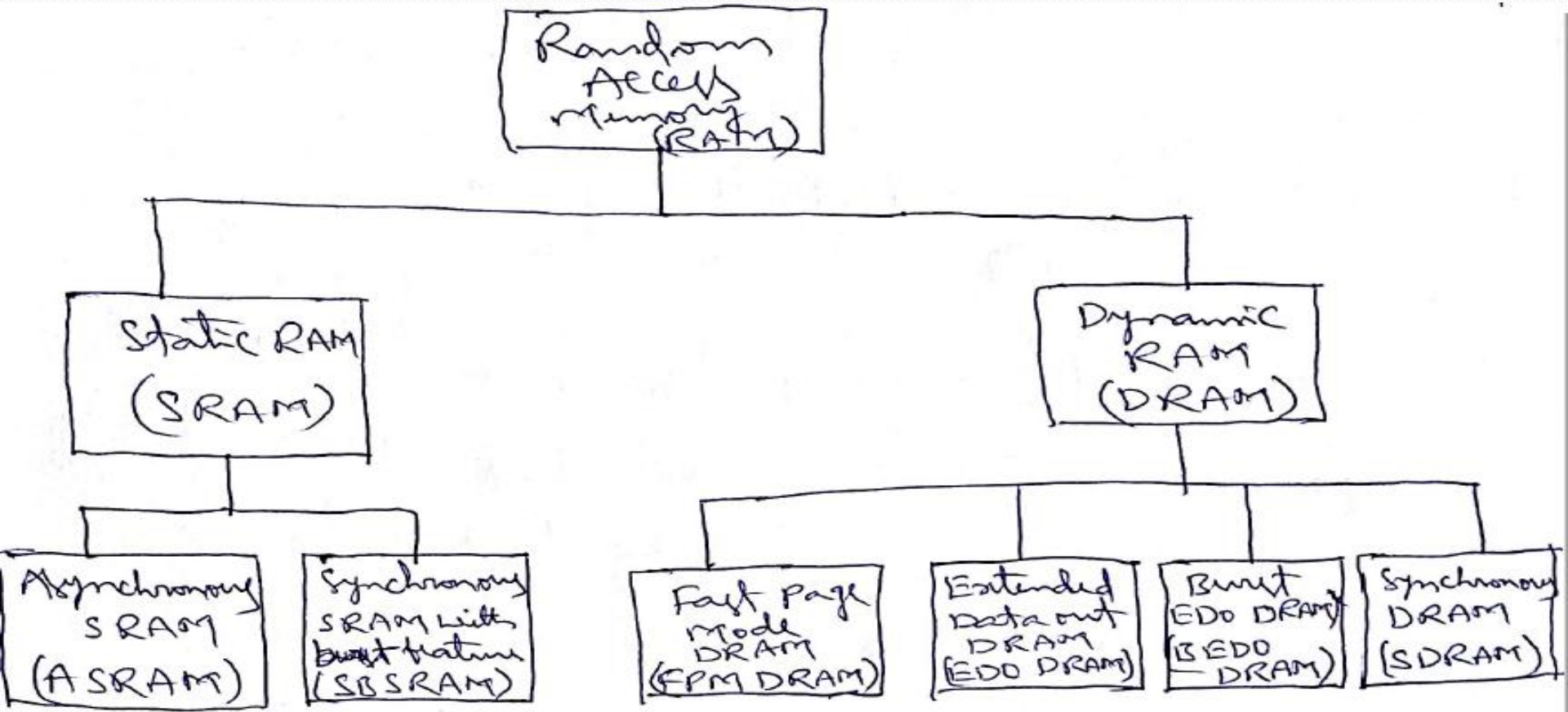


Figure 10-7. The RAM Family.

The Internal ROM organization

- To illustrate how an ICROM is structured, we use a 1024 bit device with a 256 X 4 organization.
- The logic symbol is shown in figure 10.26.

The Internal ROM organization cntd..

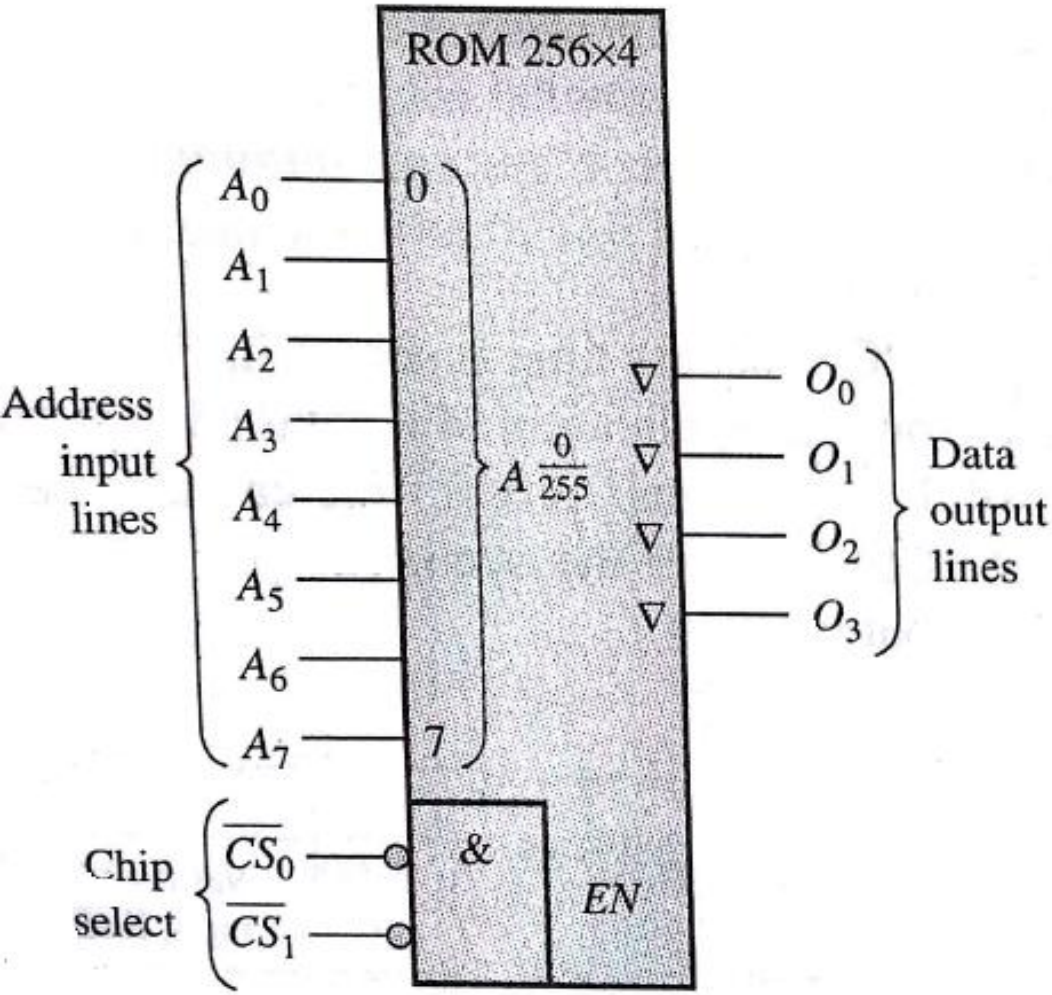


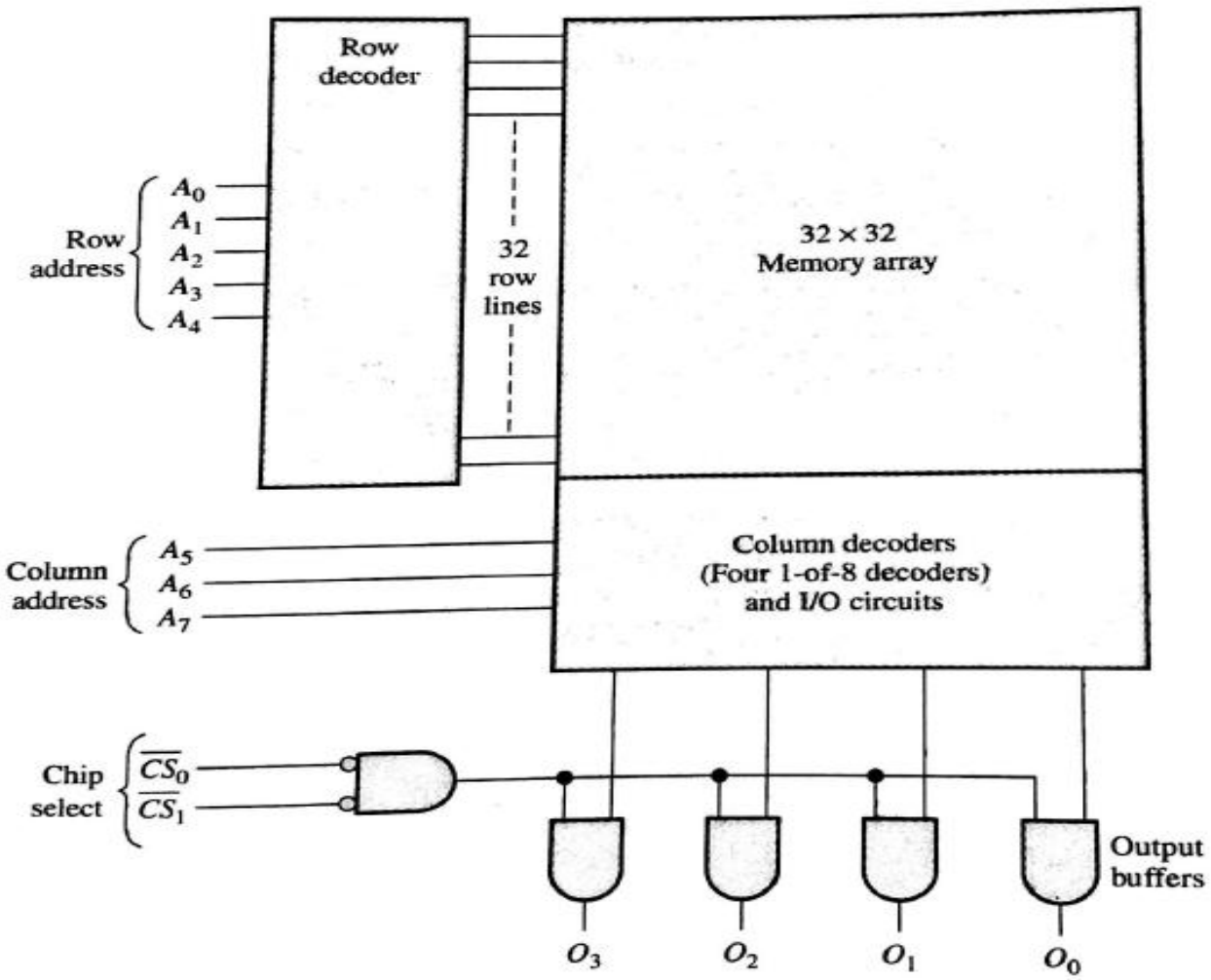
FIGURE 10–26

A 256 × 4 ROM logic symbol. The $A\frac{0}{255}$ designator means that the 8-bit address code selects addresses 0 through 255.

The Internal ROM organization cntd..

- When anyone of 256 binary codes (eight bits) is applied to the address lines, four data bits appear on the outputs if the chip select inputs are LOW.
- Although the 256 X 4 organization of this device implies that there are 256 rows and 4 columns in the memory array, this is not actually the case.
- The memory cell array is actually a 32 X 32 matrix (32 rows and 32 columns), as shown in the block diagram in figure 10.27.
- The ROM in figure 10.27 works as follows.

The Internal ROM organization cntd..



◄ FIGURE 10–27

A 1024-bit ROM with a 256 × 4 organization based on a 32 × 32 array.

The Internal ROM organization cntd..

- Five of the eight address lines (A0 thru A4) are decoded by the row decoder to select one of the 32 rows.
- Three of the 8 address lines (A5 thru A7) are decoded by the column decoder to select four of the 32 columns.
- Actually, the column decoder consists of four 1-of-8 decoders as shown in figure 10.27.
- The result of this structure is that when an 8 bit address code (A0 thru A7) is applied, a 4 bit data word appears on the data outputs when the chip select lines ($\overline{CS}0$ and $\overline{CS}1$) are LOW to enable the output buffers.

The Internal ROM organization cntd..

- This type of internal organization (architecture) is typical of IC ROMs of various capacities.

End of UNIT V